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6. AUTHORS
L. F. Velasquez-Garcia

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

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Massachusetts Institute of Technology
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14. ABSTRACT
In this project MIT designed, fabricated, and characterized massive arrays of individually ballasted silicon field emitters that use vertical ungated field effect transistors (FETs) as flow control elements to produce high current. The first design implemented arrays of field emitters with square packing. Pulsed DC tests of these devices using and external extractor resulted in 0.5 A current emission (0.5 A.cm-2), clearing showing current limitation due to the vertical ungated FETs. Spatial emission uniformity was confirmed using a phosphorous screen. The design was

15. SUBJECT TERMS
individually ballasted field emitter arrays, vertical ungated FET

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Luis Velasquez-Garcia
UU	UU	UU	UU		19b. TELEPHONE NUMBER 617-253-0730

Report Title

Integrated Vacuum Micro-Electronics for Upper Milimeter Wave Applications

ABSTRACT

In this project MIT designed, fabricated, and characterized massive arrays of individually ballasted silicon field emitters that use vertical ungated field effect transistors (FETs) as flow control elements to produce high current. The first design implemented arrays of field emitters with square packing. Pulsed DC tests of these devices using and external extractor resulted in 0.5 A current emission (0.5 A.cm-2), clearing showing current limitation due to the vertical ungated FETs. Spatial emission uniformity was confirmed using a phosphorous screen. The design was modified because the dielectric between the extractor gate and the field emitter tips was too thick, which made unfeasible to make devices with integrated extractor. MIT developed two key technologies to correct the excessive dielectric thickness. First, we changed the cross-section of the ungated FET (from round to hexagonal) and packing of the vertical ungated FETS (from square to hexagonal) to maximize the emitter density and minimize the dielectric deposition needed. Second, we developed a plasma-based planarization method. Using the modified design, were able to fabricate large arrays of individually ballasted field emitters with an integrated extractor that is very close to the emitter tips using amorphous silicon as extractor material. Unfortunately, the electrical conductivity of the extractor was too low to make the device operational. Potential solutions for this problem is ion implantation of the extractor material and use of n-amorphous silicon films or sputtered metal.

List of papers submitted or published that acknowledge ARO support during this reporting period. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Number of Papers published in peer-reviewed journals: 0.00

(b) Papers published in non-peer-reviewed journals or in conference proceedings (N/A for none)

Number of Papers published in non peer-reviewed journals:

(c) Presentations

- L. F. Velásquez-García, “System Performance Improvement Through Scaling-Down and Multiplexing,” SEDD Seminar, Army Research Laboratory, Adelphi MD, USA, December 3rd 2009.
- L. F. Velásquez-García, “High-Performance Multiplexed-Scaled Down Field-Enabled Systems,” 19th Annual CMOC Symposium, University of Connecticut, Storrs, CT, USA, April 7th 2010.

Number of Presentations: 2.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

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Peer-Reviewed Conference Proceeding publications (other than abstracts):

Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

- L. F. Velásquez-García, S. Guerrera, Y. Niu, and A. I. Akinwande, “Uniform, High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Ballasted by Vertical Si Ungated FETs – Part A: Device Design and Simulation,” submitted to IEEE Transactions in Electron Devices (2010).
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Number of Manuscripts: 2.00

Patents Submitted

Patents Awarded

Awards

Graduate Students

NAME	PERCENT_SUPPORTED
Stephen guerrera	1.00
Annie Wang	1.00
FTE Equivalent:	**2.00**
Total Number:	**2**

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
Xiaozhi Wang	0.50
FTE Equivalent:	**0.50**
Total Number:	**1**

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Akintunde Akinwande	0.10	No
FTE Equivalent:	**0.10**	
Total Number:	**1**	

Names of Under Graduate students supported

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Student Metrics

This section only applies to graduating undergraduates supported by this agreement in this reporting period

The number of undergraduates funded by this agreement who graduated during this period:	0.00
The number of undergraduates funded by this agreement who graduated during this period with a degree in science, mathematics, engineering, or technology fields:.....	0.00
The number of undergraduates funded by your agreement who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields:.....	0.00
Number of graduating undergraduates who achieved a 3.5 GPA to 4.0 (4.0 max scale):	0.00
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The number of undergraduates funded by your agreement who graduated during this period and intend to work for the Department of Defense	0.00
The number of undergraduates funded by your agreement who graduated during this period and will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields:	0.00

Names of Personnel receiving masters degrees

NAME
Akintunde Akinwande
Total Number: 1

Names of personnel receiving PHDs

NAME
Total Number:

Names of other research staff

NAME	PERCENT_SUPPORTED	
Luis F .Velasquez-Garcia	0.30	No
FTE Equivalent:	**0.30**	
Total Number:	**1**	

Sub Contractors (DD882)

Inventions (DD882)

Scientific Progress

attachment

Technology Transfer

REPORT DOCUMENTATION PAGE

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6. AUTHOR(S)

Luis Fernando Velásquez-García, Ph.D.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Massachusetts Institute of Technology, 77 Massachusetts Avenue Cambridge MA 02139

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12 a. DISTRIBUTION / AVAILABILITY STATEMENT

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12 b. DISTRIBUTION CODE

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Enclosure 1

Report Documentation Page (SF298) Continuation Sheet (Enclosure 2)

(1) Submissions or publications under ARO sponsorship during this reporting period:
  (a) Papers published in peer-reviewed journals: 0
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    i. Presentations at meetings, but not published in Conference Proceedings: 2
      - L. F. Velásquez-García, "System Performance Improvement Through Scaling-Down and Multiplexing," SEDD Seminar, Army Research Laboratory, Adelphi MD, USA, December 3rd 2009.
      - L. F. Velásquez-García, "High-Performance Multiplexed-Scaled Down Field-Enabled Systems," 19th Annual CMOC Symposium, University of Connecticut, Storrs, CT, USA, April 7th 2010.
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    iii. Peer-Reviewed Conference Proceeding publications (other than abstracts): 0
  (d) Manuscripts: 2
    - L. F. Velásquez-García, S. Guerrera, Y. Niu, and A. I. Akinwande, "Uniform, High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Ballasted by Vertical Si Ungated FETs – Part A: Device Design and Simulation," submitted to IEEE Transactions in Electron Devices (2010).
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  (e) Books: 0
  (f) Honor and Awards: 0
  (g) Title of Patents Disclosed during the reporting period: 0
  (h) Patents Awarded during the reporting period: 0

(2) Student/Supported Personnel Metrics for this Reporting Period (name, % supported, %Full Time Equivalent (FTE) support provided by this agreement, and total for each category):
  (a) Graduate Students: 2
    a. Stephen A. Guerrera, 100% supported, 100% FTE
    b. Annie I Wang, 100% supported, 100% FTE
  (b) Post Doctorates: 1
    a. Xiaozhi Wang, 50% supported, 50% FTE
  (c) Faculty: 1
    a. Akintunde I. Akinwande, 10% supported, 10%FTE
  (d) Undergraduate Students: 0

(e) Graduating Undergraduate Metrics (funded by this agreement and graduating during this reporting period): NO UNDERGRADUATES WERE INVOLVED IN THE RESEARCH

i. Number who graduated during this period: 0
ii. Number who graduated during this period with a degree in science, mathematics, engineering, or technology fields: 0
iii. Number who graduated during this period and will continue to pursue a graduate or Ph.D. degree in science, mathematics, engineering, or technology fields: 0
iv. Number who achieved a 3.5 GPA to 4.0 (4.0 max scale): 0
v. Number funded by a DoD funded Center of Excellence grant for Education, Research and Engineering: 0
vi. Number who intend to work for the Department of Defense: 0
vii. Number who will receive scholarships or fellowships for further studies in science, mathematics, engineering or technology fields

(e) Masters Degrees Awarded: 0
(f) Ph.D.s Awarded: 0
(g) Other Research staff: 1

a. Luis F. Velásquez-García, 30% supported, 30% FTE

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(4) Scientific Progress and Accomplishments (description should include significant theoretical or experimental advances): NOTHING DURING THE REPORTING PERIOD

(5) "Copies of technical reports," which have not been previously submitted to the ARO, should be submitted concurrently with the Interim Progress Report. (See page 6 "Technical Reports" section for instructions.) However, do not delay submission while awaiting Reprints of publications: WE INCLUDE IN THIS REPORT THE MANUSCRIPTS SUBMITTED TO TED.

Final report MIT Effort DARPA/MTO Hi-FIVE program

April 21st 2008 – October 20th 2010

0. Introduction

Field emission of electrons consists of two processes, i.e., (i) *transmission of electrons* (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by the application of a high electrostatic field[1], and (ii) *supply of electrons* from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the FEA.

Transmission-limited field emission: In this case, the emitted current is described by the Fowler-Nordheim (FN) equation, which relates the current density to the electrostatic field at the surface of the emitter tip and the work function of the tip. $I_E(V_G)$, i.e., the current emitted from a tip biased at a voltage V_G is

$$I_E\left(V_G\right) = A_{tip}\,\frac{1.27\times10^{-6}}{\phi}\cdot\,\beta^2\cdot V_G^2\cdot\exp\left[\frac{9.87}{\sqrt{\phi}} - \frac{6.53\times10^{7}\cdot\phi^{3/2}}{\beta\cdot V_G}\right]\text{(A)} \qquad (1)$$

where α_{tip} (cm^2) is the emitting area of the tip, ϕ (eV) is the workfunction of the tip, and β (cm^{-1}) is the field factor of the emitter

$$\beta = \frac{k_F}{r^n}\ (\text{cm}^{-1}) \qquad (2)$$

where $k_F \approx 2.5\times10^6$, $n \approx$ 0.69-0.8, and r (nm) is the tip radius[2]. A surface electrostatic field of about 3×10^7 $V.cm^{-1}$ is required to produce field emission. As shown in Eq. 1, field emitted current has an exponential dependence on the field factor and the workfunction; therefore, field emission is extremely sensitive to tip radii variation and workfunction variation:

- Changes in the workfunction are mostly related to absorption/desorption of gases by the tip, causing current emission with temporal non-uniformity. Therefore, emitters made of high workfunction materials have better temporal stability.
- Tip radii variation across the FEA are mainly related to fabrication variability, causing current emission with spatial non-uniformity. The tip radii spread is related to the magnitude of the nominal tip radius. Based on Eq. 2, it is highly desirable to implement FEAs with emitters as sharp as possible to produce high electrostatic fields with low voltage. Unfortunately,

nanometer-sized tip radii in FEAs have a distribution with large spread[3], which results in severe spatial non-uniformity. The standard deviation of emitters with nano-sized tip radii is typically as large as 53% the average tip radius[2]. However, arrays of isolated CNTs with 24.5 nm average tip radius typically have less than 4% standard deviation[4]. Therefore, optimization of the FEA should result in emitter tip radii with near monochromatic distribution while still turning-on at low voltage.

Supply-controlled field emission: The conventional approach to attain uniform electron emission from supply-limited FEAs has been through the use of large feedback resistors in series with the field emitters. However, this approach is unattractive because current uniformity is achieved at the expense of the current level. A better approach would involve a device that has current source-like behavior to simultaneously provide high current and high dynamic resistance to each emitter. In order to achieve high-current emission with high temporal and spatial uniformity, we proposed to use massive arrays of gated field emitters where each field emitter individually controlled by a vertical ungated FET[5] (Figure 1).

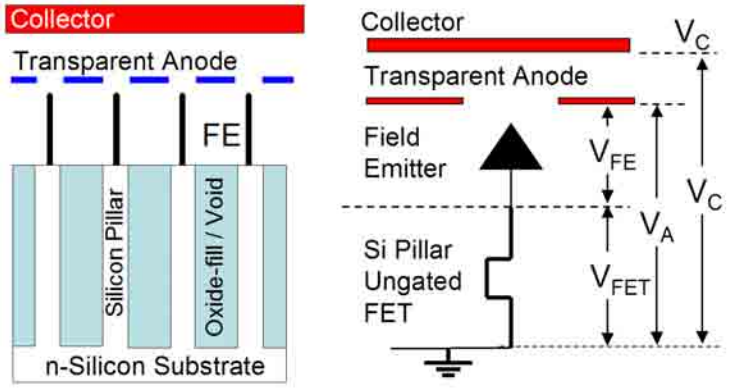

Figure 1 *Device structure (left) and equivalent circuit (right). Each field emitter is fabricated on top of a different silicon column (i.e., ungated FET). The bias voltage V_A is divided between the voltage across the FE (V_{FE}) and the voltage across the FET (V_{FET}).*

An ungated FET acts as current source, effectively providing high current with high dynamic resistance for voltage drops across the FET larger than the saturation voltage. The FET achieves current source-like behavior due to the velocity saturation of carriers in the semiconductors, as well as the high aspect-ratio of the channel (the channel pinches-off due to the high electrostatic field). Individual control of the supply of electrons of each emitter prevents destructive emission from the sharper tips while allowing higher overall current emission because of the emission of duller tips. One can readily show that the current through and FE/FET unit (when the FET is operating in its saturation regime) is equal to the implicit function

$$I_E(V_G) = A_{tip}\frac{1.27\times10^{-6}}{\phi}\cdot\beta^2\cdot\left(V_G - V_{DSS} - \left(I_E - I_{DSS}\right)\cdot r_{out}\right)^2\cdot\exp\left[\frac{9.87}{\sqrt{\phi}} - \frac{6.53\times10^7\cdot\phi^{3/2}}{\beta\cdot\left(V_G - V_{DSS} - \left(I_E - I_{DSS}\right)\cdot r_{out}\right)}\right] \text{ (A)} \quad (3)$$

where I_{DSS} (A), V_{DSS} (V), and r_{out} are the saturation current, saturation voltage, and output resistance of the FET, respectively. The current uniformity in an FEA can be benchmarked using a sensitivity parameter, i.e., a measure of the variation in the current emission due to fluctuations in the workfunction and the tip radii. The sensitivity S of the FE/FET unit is

$$S = S_\phi + S_r = \frac{1}{I_E}\frac{dI_E}{d\phi}\Delta\phi + \frac{1}{I_E}\frac{dI_E}{dr}\Delta r \approx 2\frac{I_{MAX} - I_{MIN}}{I_{MAX} + I_{MIN}} \quad (4)$$

where S_f and S_r are the current sensitivities with respect to the variations in the workfunction and the tip radius, $\Delta\phi$ and Δr are the variations in workfunction and tip radius, and I_{MAX} and I_{MIN} are the maximum and minimum emitter currents, respectively. From Eq. 4, it is clear that the specifications of the ungated FETs are less stringent if the emitter tip radii spread is as small as possible. One can readily show through simulations that by implementing a suitable FE/FET unit, it is possible to arbitrarily reduce the sensitivity of the FEA to changes in the work function and/or tip radii variation. For example, an FE/FET unit using a total bias voltage V_G of 100 V was, with $\alpha_{tip} = 0.4\pi\cdot r^2$, r_o = *30 nm*, Δr = *1.5 nm (i.e. 5% r_o)*, ϕ = *4.8 eV*, $\Delta\phi$ = *0.2 eV*, I_{DSS} = $1\mu A$, can achieve good current uniformity with output resistances r_{out} equal to 100MΩ or more.

1. First Cathode Design, Fabrication, and Characterization

The objective of the first phase of the project was to demonstrate high current emission from a massive array of field emitters individually controlled by vertical ungated FETs with the following specs:

Milestones

Phase 1	
6 months	Demonstrate current density of 0.1 A cm^{-2}.
	Demonstrate a total current of 0.25 A
12 months	Demonstrate current density of 1 A cm^{-2}.
	Demonstrate beam compression of 20:1 by Simulation
18 months	Demonstrate current density of 20 A cm^{-2}.
	Experimentally demonstrate beam aspect ratio of 20:1
	Demonstrate current of 250 mA

Based on previous modeling and experimental results using 100:1 FET test structures with

square packing and 10^{13} – 10^{15} cm^{-3} doping concentration, we designed and proposed a fabrication process flow for uor cathode. The highlights are:

- 4-6 Ohm.cm wafers (3 μA per FET with 30:1 – 50:1 columns ~ 1 μm wide)
- Square emitter packing, 4 μm emitter pitch
- Projection photolithography in the key steps (more uniform arrays)
- Array sizes include the compression ratio required by the program. The die layout is shown in Figure 2. A summary of the specs of each array part of the die layout appears in Table 1.
- Integrated gates. Both single and double gate versions

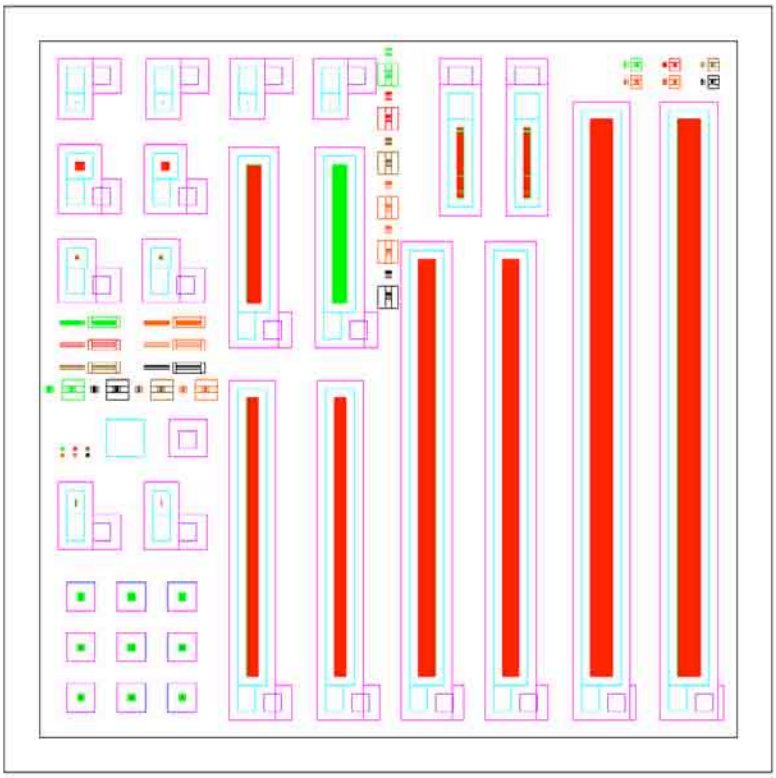

Figure 2 *Die layout.*

The proposed fabrication process flow for the structures is shown in Figure 3, while selected views of the process flow in progress are shown in Figure 4. As it will be explained in the next section, we found fabrication problems while trying to complete the proposed fabrication process flow. Meanwhile, 1-cm^2 arrays with 100:1 FETs and 10 μm emitter pitch were used to demonstrate high and uniform current. A block diagram of the pulsed test rig is shown in Figure 5. It is composed of the individually ballasted FEA, an unaligned perforated grid separated by a polymer gasket, and an external collector. In the pulsed test rig the FEA is connected to the ground through a resistor R_M that is used to determine the current emitted by

the FEA. The grid voltage is supplied by a Glassman EQ1R1200 power supply that is controlled by a DEI PVX-4140 pulse generator. The collector electrode voltage is supplied by a Glassman LH3R1.721 power supply. Pulses of 2 μs with a period of 10 s were used to energize the grid. We verified that the pulse duration is long enough to produce a steady-state response from the FEAs, while the square wave period is long enough to substantially decrease the impact of the grid heat dissipation. We also verified the linearity between the collector current and the emitted current.

Size X	Size Y	Ratio Emitting Area	# emitters	Full dimensions with gates (mm)	Total Current (A)	# arrays in Die
80	2000	25	160,00	9 X 0.82	4.80E-01	2
60	1500	25	90,000	7 X 0.74	2.70E-01	2
40	1000	25	40,000	5 X 0.66	1.20E-01	2
50	500	10	25,000	3 X 0.7	7.50E-02	2
25	250	10	6,250	2 X 0.6	1.88E-02	2
30	30	1	900	1.12 X 0.62	2.70E-03	2
10	10	1	100	0.54 X 0.54	3.00E-04	2
1	25	25	25	1.1 X 0.54	7.50E-05	2
3	3	1	9	0.7 X 0.54	2.70E-05	2
1	1	1	1	0.7 X 0.54	3.00E-06	2

Table 1. *Array sizes (square packing)*

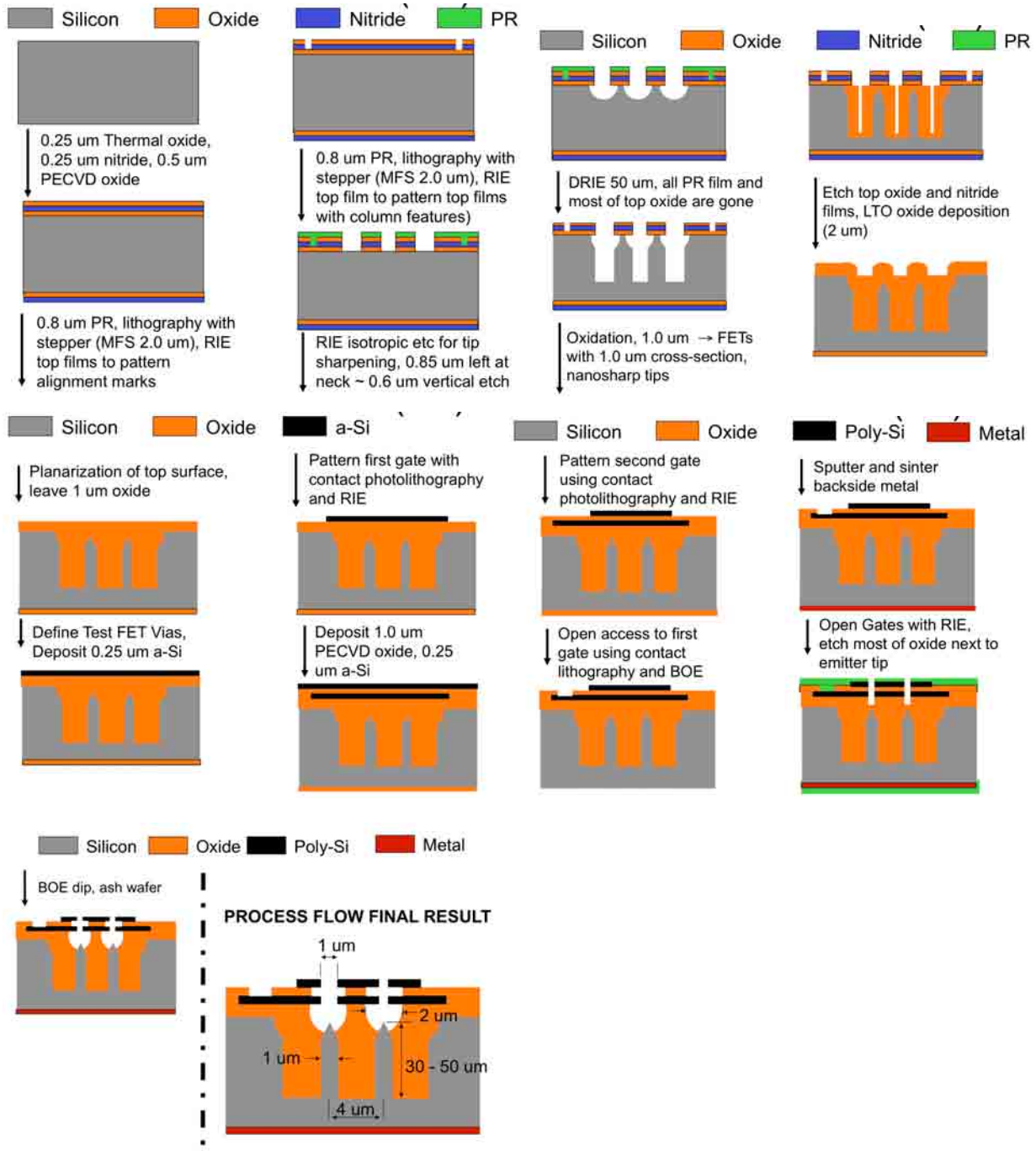

Figure 3 *Proposed fabrication process flow. Flow sequence within diagram is top to bottom, left to rigth, while flow between diagrams is left to right, top to bottom.*

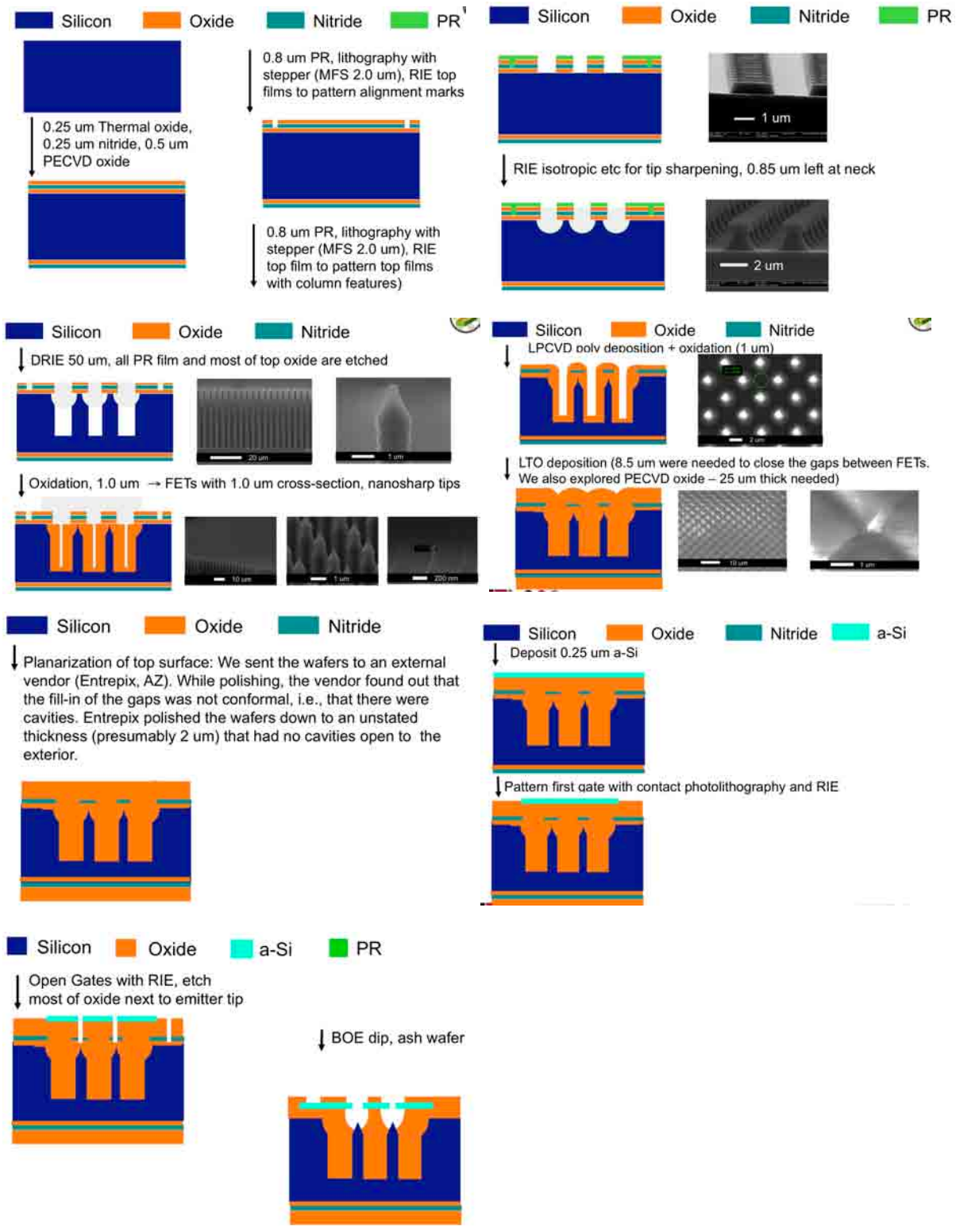

Figure 4. *Selected fabrication fabrication results. Flow sequence within diagram is top to*

bottom, left to rigth, while flow between diagrams is left to right, top to bottom.

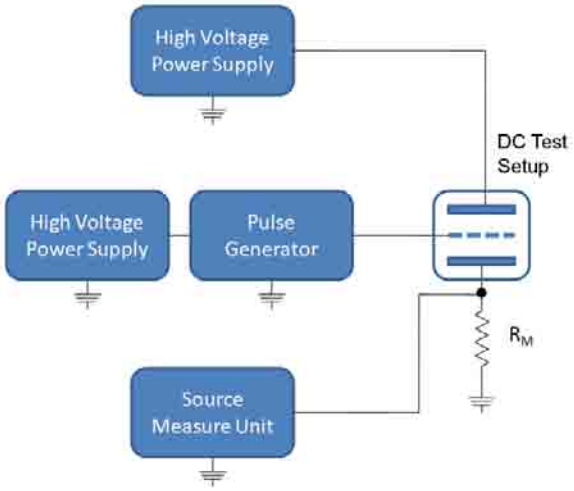

Figure 5. *Block diagram of the pulsed DC setup.*

Figure 6-A is a plot of the DC and pulsed IV characteristics of a 1-million array of field emitters individually ballasted by ungated FETs that was fabricated on a silicon substrate with a resistivity of 34.7 Ω.cm (doping concentration of 1.25×10^{14} cm^{-3}). The maximum emitted current per tip is 0.48 uA assuming uniform operation of the FEA. This is consistent with the maximum current I_{MAX} = 0.4 uA obtained at a bias of 100 V from simulations of the FET. The FN plot of the emitted current obtained from both DC and pulsed tests is shown in Figure 6-B. The plot clearly shows that for high grid voltage, the emission current is electron supply limited whereas for lower applied grid voltages the emission current is barrier limited. In the electron supply limited regime, the emitted current of 0.48 A is consistent with the saturation current of the ungated FET is one allows for the finite output resistance of the ungated FET. From the section of the FN plot for which electron emission is barrier limited, we estimated a field factor equal to 2.26×10^{5} cm^{-1} using 4.05 eV as the workfunction for Si; the field factor corresponds to a tip diameter of 32.5 nm if one uses Eq. 2 with $k_F = 2.5\times10^{6}$ and n = 0.69. The radius estimate is consistent with the tip radius of 42 nm from SEMs.

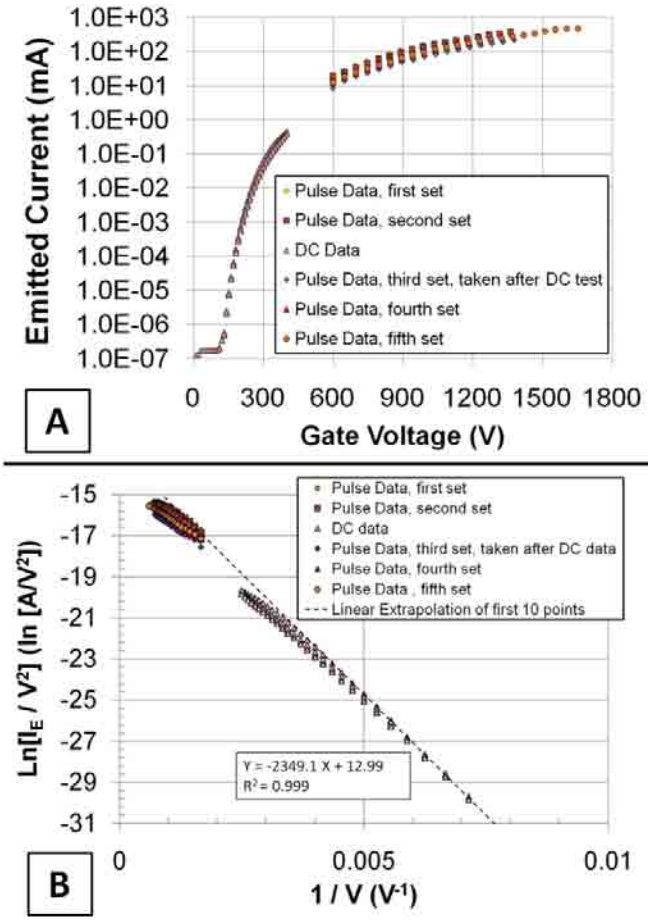

Figure 6. *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made of silicon with a resistivity of 34.7 Ω.cm: IV characteristics (A), FN plot of the emission current (B).*

Figure 7-A is a plot of the DC and pulsed IV characteristics for an array of 1-million field emitters individually controlled by vertical ungated FETs that was fabricated on a substrate with a resistivity of 178 Ω.cm (doping concentration of 2.4×10^{13} cm^{-3}). The emission current saturates at 0.109 A at grid voltages above 1200 V. The maximum emission current per tip is 109 nA, which is a factor of 5 larger than the 20 nA saturation current from simulations of the FET. Given the output conductance of the ungated FET, it is expected that the emission current will vary with the voltage drop across the ungated FET especially for the sharper tips. It is not clear at this time if this would account for the almost factor of 5 larger emission current per tip than the simulated ungated FET. Another potential source of additional current for the ungated FET is impact ionization at the drain region of the ungated FET due to the high voltage between the source and the drain. Also, impurity segregation into the silicon channel is expected to increase the channel doping, which should substantially increase the carrier concentration in lowly-doped

substrates. The FN plot of the emitted current obtained from both the DC and pulsed tests is shown in Figure 7-B. At low voltages, the slope of the FN plot is constant and negative, corresponding to the region dominated by electron transmission through the barrier. However, the slope becomes positive at high voltages (> 1200 V) corresponding to the region dominated by electron supply to the barrier, as previously shown by Hong et al for FEAs ballasted by a MOSFET [4]. From the region in which electron emission is controlled by transmission through the barrier we extracted field factor equal to 2.73×10^{5} cm^{-1}, which corresponds to a tip radius if 24.8 nm if we use Eq. 2 with $k_F = 2.5 \times 10^6$ and $n = 0.69$. This is consistent with the tip radius of 33 nm from the SEMs.

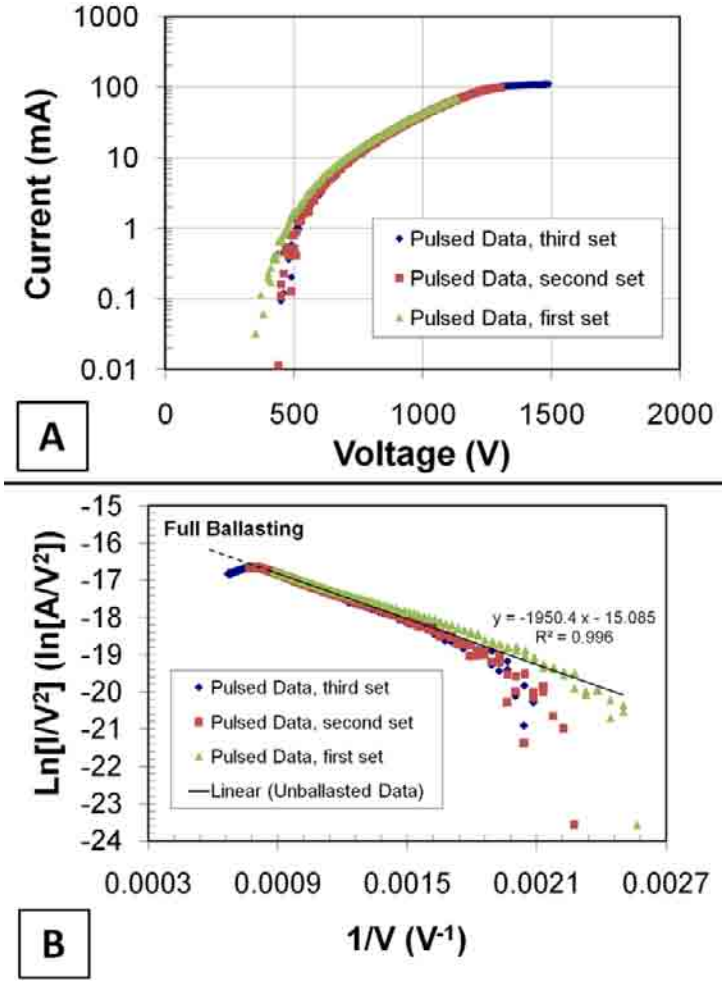

Figure 7. *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made of silicon with a resistivity of 178 Ω.cm: IV characteristics (A), FN plot of the emission current (B).*

To corroborate the results and conclusions from the IV characterization, a series of tests that involved a phosphor screen were conducted (Figure 8) The phosphor screen was biased at 1100

V and suspended about 1 cm from the FEA. The current transmitted by the grid hits the phosphor screen, which produces photons that can be captured using a camera. We used a Nikon D70 camera with a 28-85 mm F 3.5-4.5 lens and we took pictures with 30 s exposure. The images indicate that at low-current level, the emission starts at specific locations on the FEA surface. With increasing bias voltage, spatial uniformity is achieved, even at relatively low currents (~ 400 uA). Based on the experimental IV characteristics we believe that a small fraction of the FEA is active, but based on the phosphor screen tests we believe that the active FET/FEs are roughly evenly distributed across the FEA.

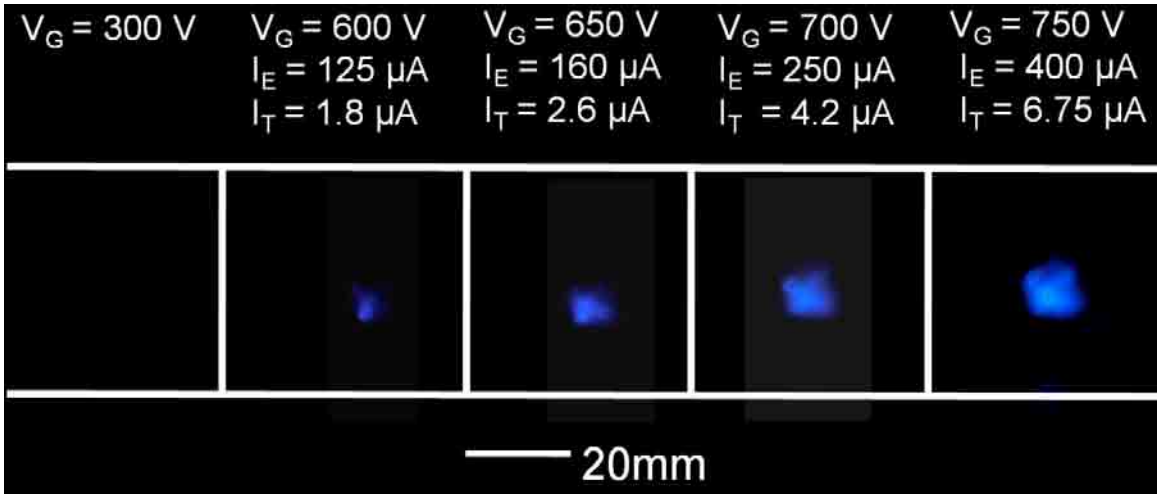

Figure 8. *Series of optical pictures at different emission currents in the phosphor screen test. For each picture the bias grid voltage VG, the emitted current IE, and the transmitted current IT (which is collected by the phosphor screen) are provided as guidance.*

2. Fabrication difficulties first design

The objective of the project was to demonstrate high current from field emission cathodes composed of a massive array of individually ballasted field emitters using vertical ungated FETs. The cross-section of the proposed cathode is shown in Figure 8. By October 20th 2009, i.e., the start of the NCE, the fabrication of the first batch of devices with an integrated single gate was completed. The devices were high aspect-ratio arrays of individually ballasted silicon field emitters with square packing (Figure 9).

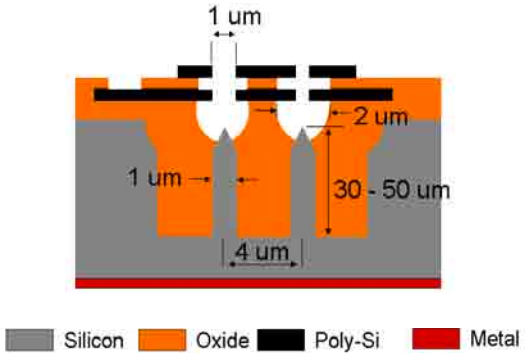

Figure 8. *Cross-section schematic of an individually ballasted FEA.*

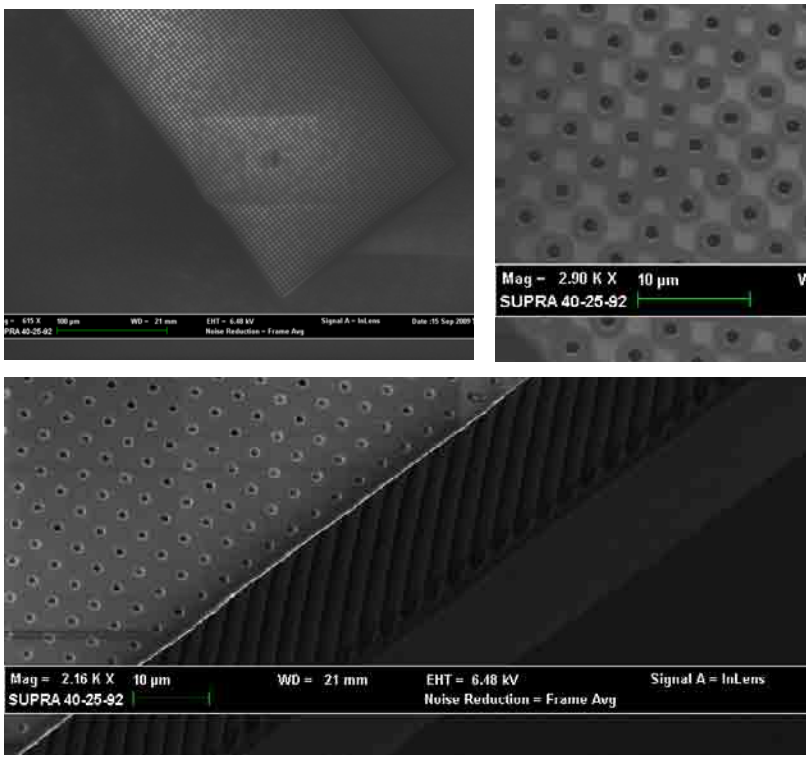

Figure 9. *Global top view (top left), top view detail (top right), and cross-section (bottom) of the fabricated field emitter array cathodes.*

Even though the field emitters on top of the ungated FETs were very sharp (Figure 10), metrology of the cross section of the devices revealed that the devices were not functional because the dielectric between the first gate and the emitters was visibly thicker than previously thought (Figure 11). This is a result of the emitter packing implemented and the conformality of the dielectric films used. In order to have working devices, a re-design of the emitter packing to reduce the amount of non- conformal deposition of dielectric was needed.

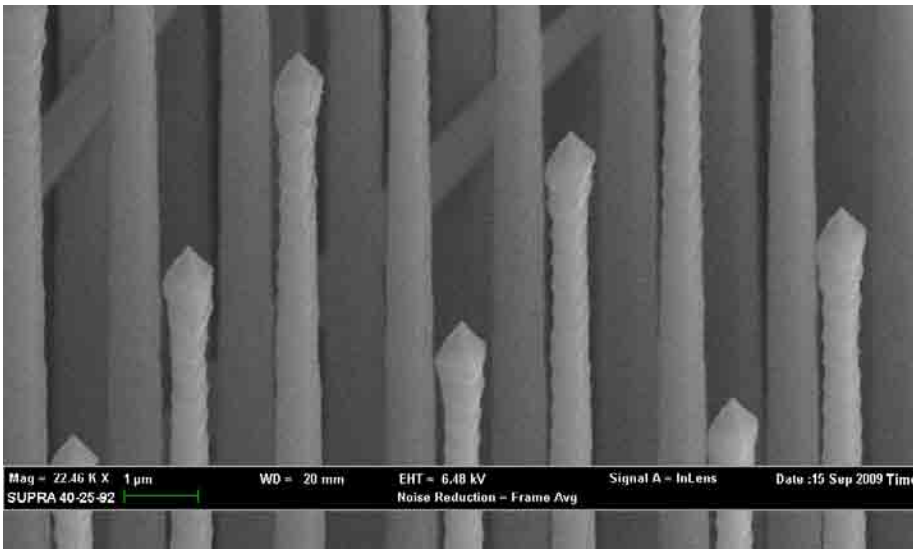

Figure 10. *An array of individually ballasted filed emitters without the integrated gate.*

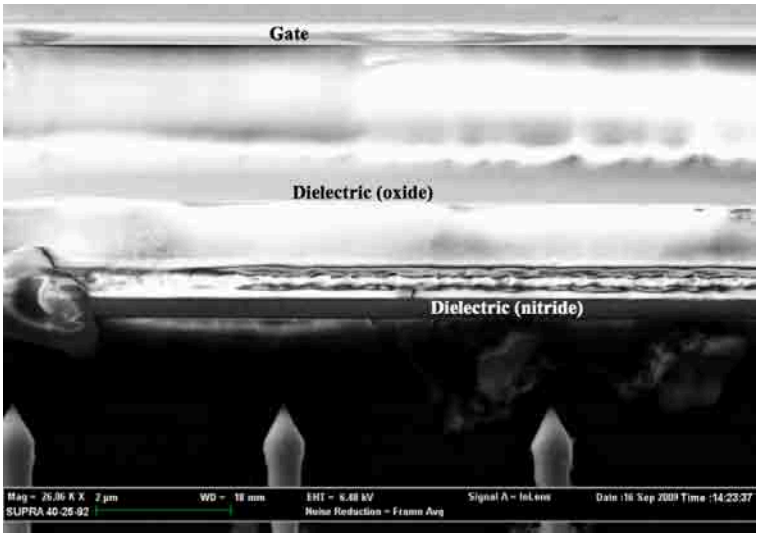

Figure 11. *Cross-section of an individually ballasted field emitter array with integrated extractor.*

3. Research conducted to obtain working devices since the beginning of NCE

In a Cartesian array the elements are located at the four nodes of a square. In our case, the elements of the array are the individually ballasted field emitters, i.e., a field emitter on top of a high aspect ratio silicon column. The square packing creates problems when we try to fill-in the gaps between the elements of the array. In a square packing, the diagonal between opposite element is 41% larger than the distance between adjacent elements. Therefore, conformal filling-

in of the gaps results in voids when the adjacent elements meet (Figure 12, left). Based on our process flow, the 41% extra oxide deposition needed to completely fill-in the gaps requires using non-conformal deposition methods such as LTO and PECVD, resulting in dielectric layers that are unnecessarily separate the field emitters from the proximal gate. However, in a hexagonal packing (Figure 12, right) each element is equidistant to all adjacent elements and therefore, the interstitial voids are visibly smaller. A hexagonal packing is also the densest, with a net increase of 15% in the element area density. If the elements are hexagonal, then the interstitial voids can be further reduced. Therefore, a mask set that introduces hexagonal packing of hexagonal columns was designed (Figure 13).

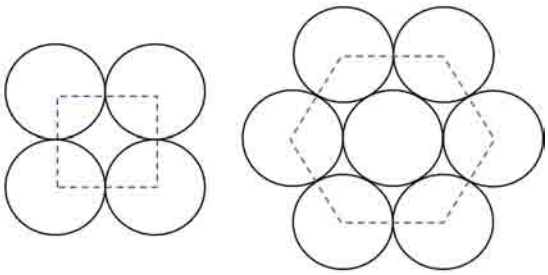

Figure 12. *Unit cell of an array with square packing (left) and with hexagonal packing (right).*

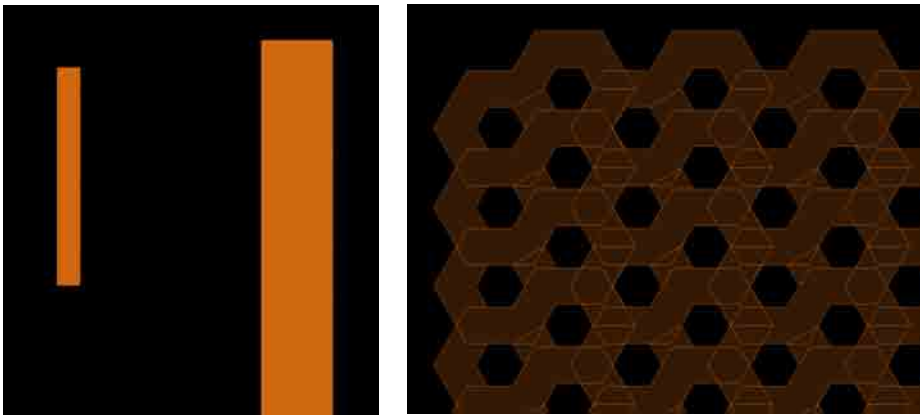

Figure 13. *Modified device layout (column level) that implements hexagonal columns with hexagonal packing.*

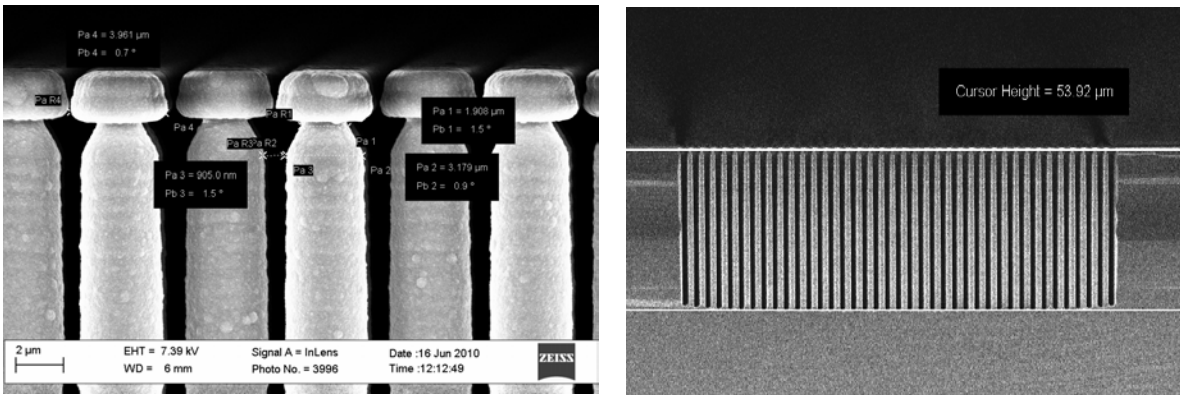

Figure 14. *Cross-section of the individually ballasted field emitters after DRIE.*

Using the modified layouts we attempted the fabrication of the devices. In our fabrication process flow, the field emitters are partially etched with isotropic plasma and the silicon columns (the high aspect ratio ungated FETs that individually control each field emitter) are etched using DRIE (Figure 14). Then, thermal silicon oxide is grown on the columns to achieve a certain silicon column aspect ratio and to fully sharpen the silicon field emitters (Figure 15). After that, a conformal layer of LPCVD polysilicon is deposited that is then oxidized to fill-in the gaps between the columns (Figure 16). By the end of the second oxidation, and inter-column gap of 400 nm remained. Finally, 1 micrometer of LTO oxide was deposited to cover the features. For comparison, the original layouts with square packing required 10 um of LTO deposition to achieve the same result. A micron-level roughness is present on the wafer after the LTO deposition.

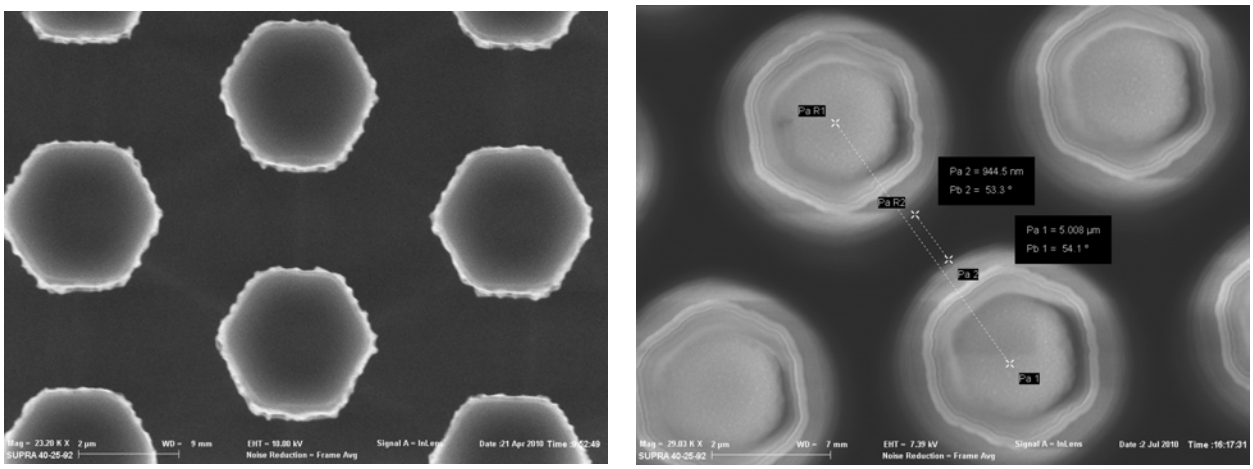

Figure 15. *Top view of Si column before (left) and after (right) wet oxidation.*

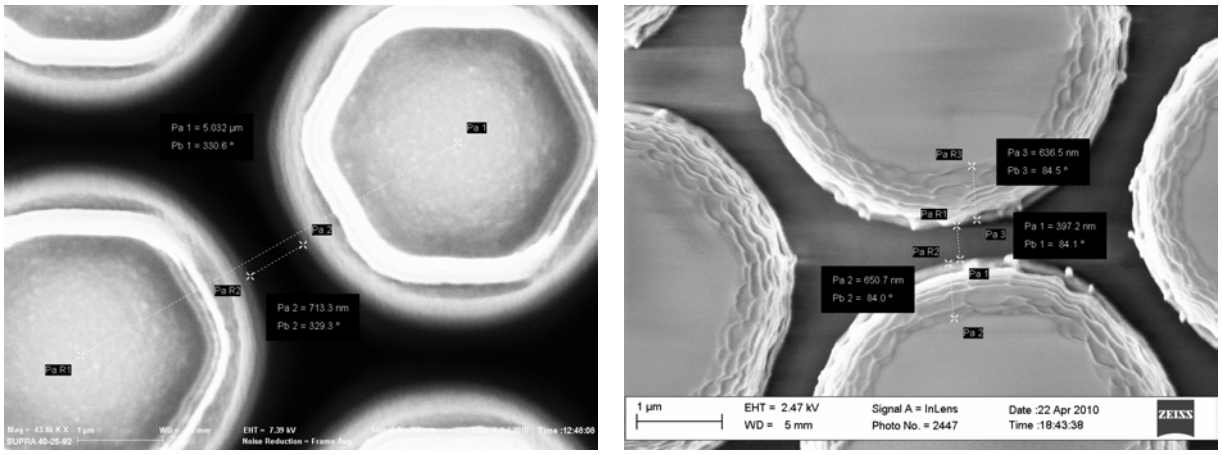

Figure 16. *Top view of Si columns after Poly-Si deposition (left) and after wet oxidation of Poly-Si (right).*

After the fill-in of the space between the columns, two strategies for planarization of the substrate have been explored. The first approach involves using CMP. During the NCE we bought a new CMP from a DoD DURIP. We installed the machine (Figure 17) and we are characterized its performance while developing recipes to planarize substrates coated with oxide and polySi (Figure 18).

Figure 17. *Front view of the installed CMP (left) and detail of the polishing pad (right).*

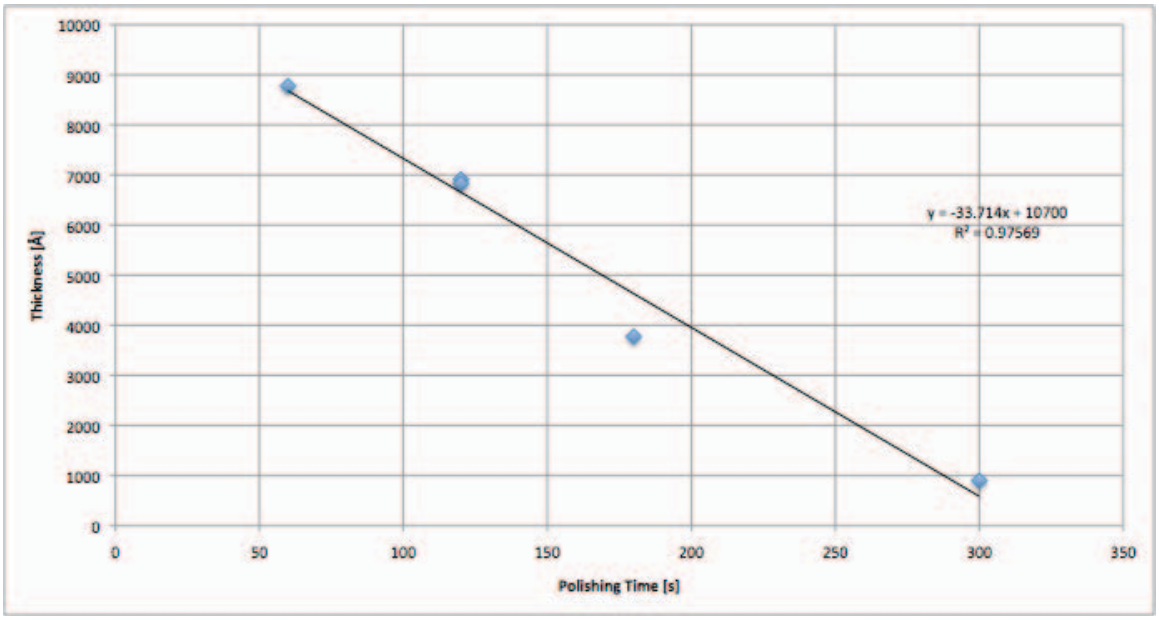

Figure 18. *Film thickness vs. time. An average etch rate of 34 Å/s was obtained.*

As a parallel approach, we explored a plasma-based approach for planarization. To planarize the wafer, a O_2/CH_3 plasma chemistry was developed, in which O2 is intended to etch photo-resist and CH3 to etch oxide. The wafer is coated with PR and then planarization of the wafer sis attempted using plasma. Our best results come from using an O_2:CH_3 mixture is 6:11. AFM characterization of the substrate evidences planarization better than 200 nm (Figure 19).

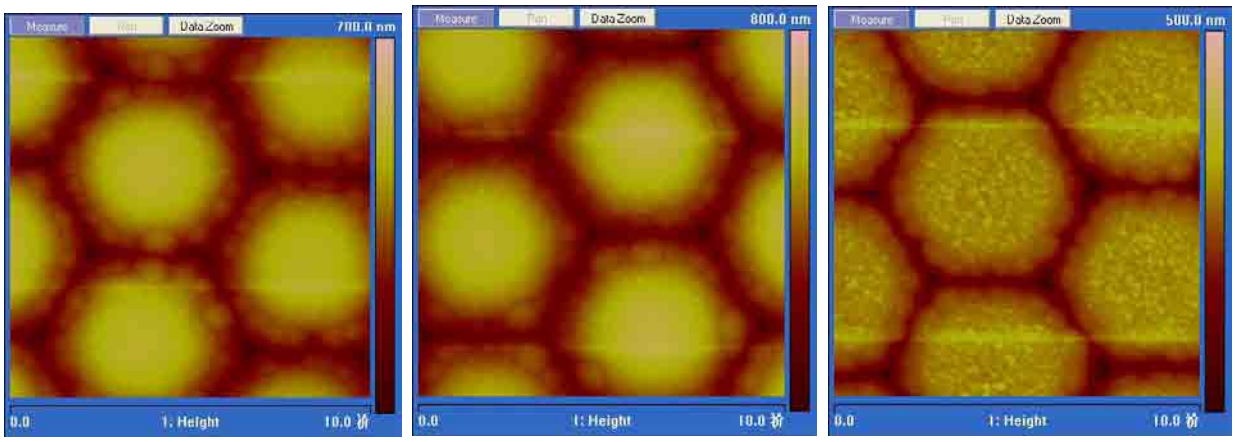

Figure 19. *AFM characterization of the plasma planarization technique with 300 s (left), 600 s (center), and 900 s (right) etch time.*

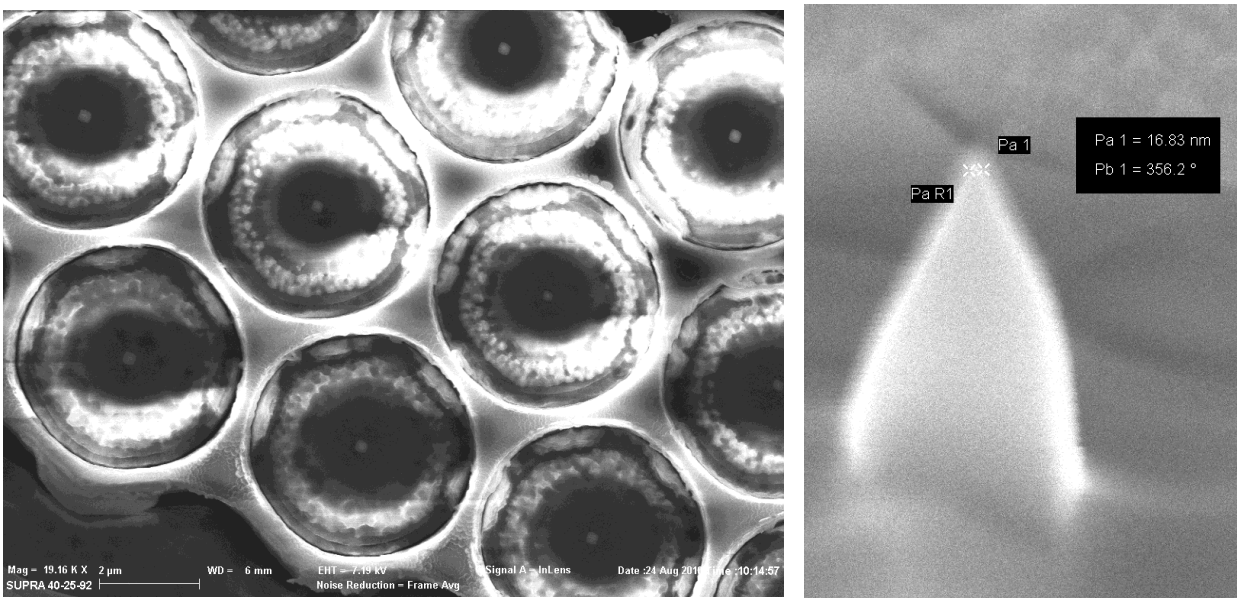

Figure 20. *Fabricated field emitter array (left) and emitter tip detail (right).*

Using the hexagonal column-hexagonal packing array technology and the plasma planarization technology, we were able to fabricate devices with an integrated gate that had a visibly smaller separation (~1-2 µm) and visibly sharper tips -about 8 nm of tip radius (Figure 20). We were not able to test the devices because we detached the integrated gate in the final BOE etch that completes the emitter tip release (Figure 21).

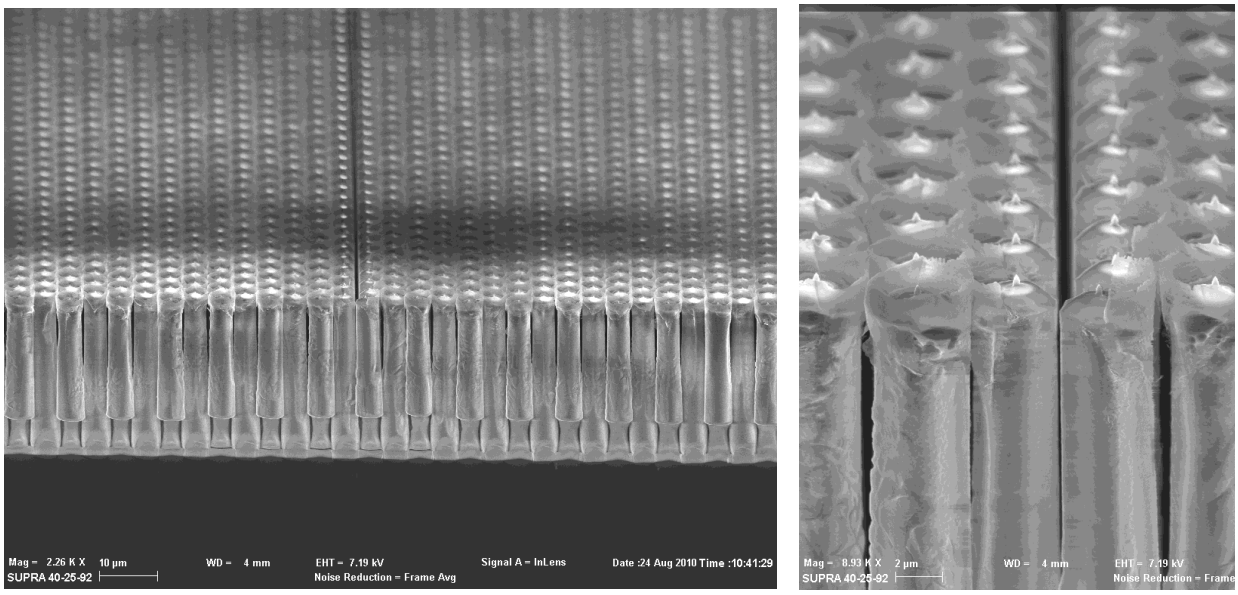

Figure 21. *Cross-section of fabricated cathode after BOE final release (left) and detail of the field emitters. From the picture, it is clear that the plasma planarization brings the gate level very close to the emitter tip.*

We corrected the fabrication problems we pointed out and were able to make field emitter arrays with integrated gate that is at the level of the field emitter tips (Figure 22). However, we were not able to obtain new data because the electrode material was not conductive enough (the extractor was made of amorphous silicon)

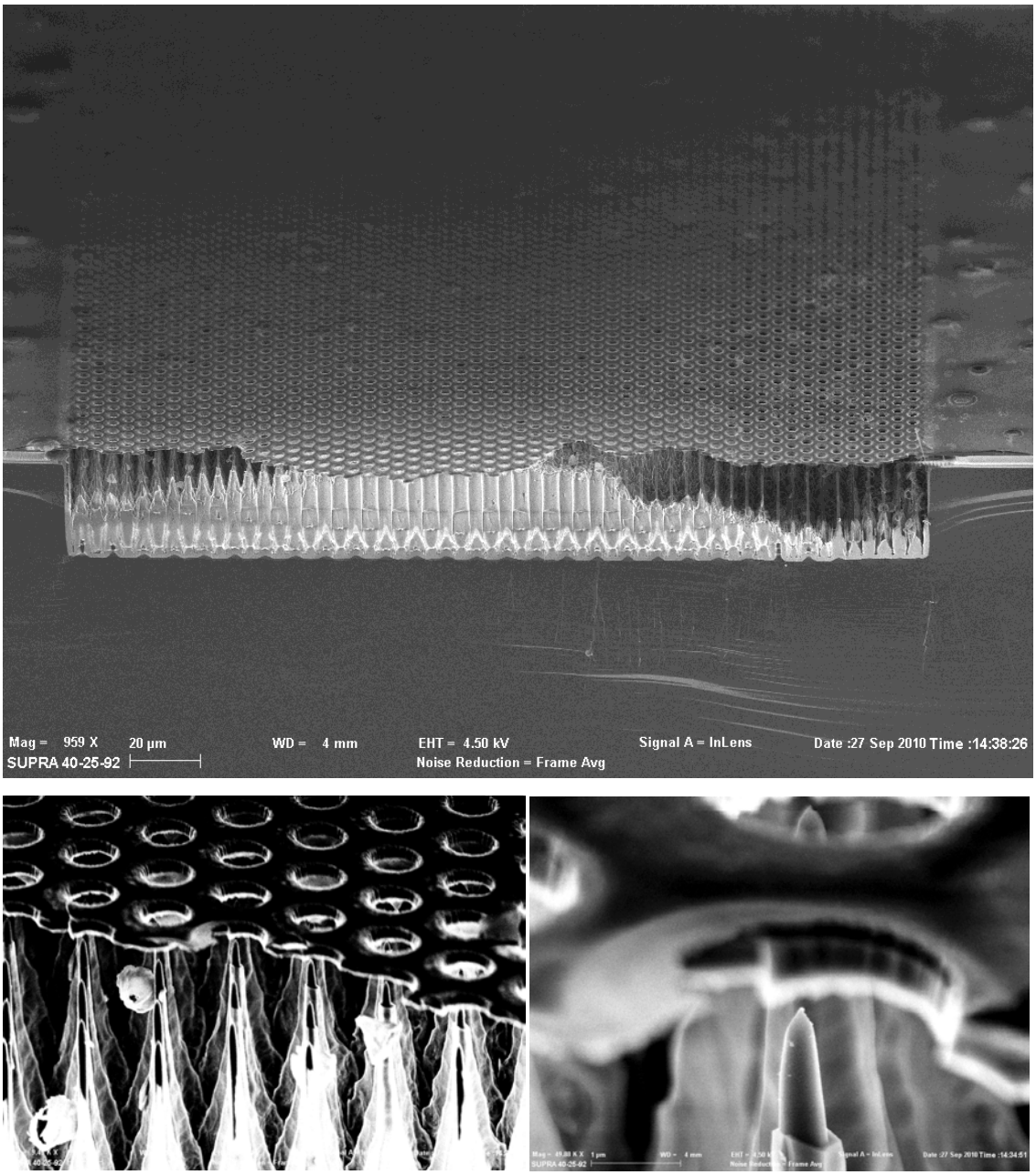

Figure 22. *Cross-section of fabricated cathode after BOE final release (top) and detail of a few field emitters (bottom left) and single emitter (bottom right). Nanosharp field emitters with self-aligned extractor at the level of the emitter tip were successfully fabricated.*

4. Future work

The results of this project are very encouraging. We were able to demonstrate high and uniform current emission (0.5 A) from field emission cathodes using massive arrays of field emitters that are individually controlled by vertical ungated FETs. We were also able to fabricate cathodes with integrated extractor electrode that is at level with the emitter tips. However, the electrical conductivity of these devices was too low to yield working devices. We believe this can be solves by changing the electrode material to n-amorphous silicon or metal. We strongly recommend further funding this line of research, as it is our opinion that groundbreaking results are at reach.

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Submitted manuscripts:

- L. F. Velásquez-García, S. Guerrera, Y. Niu, and A. I. Akinwande, "Uniform, High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Ballasted by Vertical Si Ungated FETs – Part A: Device Design and Simulation," *submitted to IEEE Transactions in Electron Devices* (2010).
- L. F. Velásquez-García, S. Guerrera, Y. Niu, and A. I. Akinwande, "Uniform, High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Ballasted by Vertical Si Ungated FETs – Part B: Device Fabrication and Characterization," *accepted for publication, IEEE Transactions in Electron Devices* (2011).

Uniform High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Controlled by Vertical Si Ungated FETs – Part A: Device Design and Simulation

Luis F. Velásquez-García, Senior Member, IEEE, Stephen A. Guerrera, Ying Niu, and Akintunde I. Akinwande, Fellow, IEEE

***Abstract*—In this paper we report the design and simulation of electron sources composed of arrays of Si field emitters that are individually ballasted by a current source. Each field emitter is fabricated on top of a vertical ungated field effect transistor (FET), a two-terminal device based on a very high aspect-ratio Si column. The ungated FET takes advantage of the velocity saturation of electrons in silicon, the high aspect-ratio of the ungated FET, and the doping concentration of the semiconductor to achieve current source-like behavior. The proposed technology can be used to implement cathodes capable of reliable uniform and high current emission.**

***Index Terms*—Ballasting, cathodes, electron supply control, Si field emission arrays, vertical ungated Si FETs.**

I. INTRODUCTION

Most commercially available electron sources are based on thermionic emission in which electrons are "boiled" off the surface of metals or semiconductors when the thermal energy of the electrons is sufficient to overcome the potential barrier holding the electrons within the material [1]. Even though thermionic cathode technology has been quite successful, thermionic-based cathodes require high vacuum (> 10^{-5} Torr) and high temperature (> 2000 K) to operate, which results in inefficient power consumption, poor reliability, and portability constraints. The demand for more efficient electron sources has driven the research of cold cathode technologies, particularly field emission. Field emission arrays (FEAs) are potential cold cathodes that could be used in a variety of vacuum micro- and nano-electronic device applications such as field emission displays (FEDs), high frequency amplifiers, gas ionizers, X-ray sources, and multi-electron beam lithography [2]-[7]. In the majority of these applications current level, stability, reliability, lifetime, and emission uniformity are the key metrics for cathode performance.

Field emission of electrons from metal or semiconductor surfaces consists of two processes, i.e., (i) *transmission of electrons* (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by the application of a high electrostatic field [8], and (ii) *supply of electrons* from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the field emitter (FE). Control of the transmission process to produce high uniform current from FEAs has largely been unsuccessful due to the physics of the field emission process. The Fowler-Nordheim (FN) equation relates the current density to the electrostatic field and the work function. $I_E(V_G)$, i.e., the current emitted from a tip biased at a voltage V_G is [9]

$$I_E(V_G) = \alpha_{tip} \frac{A_{FN}}{\phi t^2(y)} \cdot E_{local}^2(V_G) \exp\left[\frac{-B_{FN} \cdot \phi^{3/2}}{E_{local}(V_G)} v(y)\right] \text{(A)} \qquad (1)$$

where α_{tip} (cm^2) is the emitting area of the tip, ϕ (eV) is the workfunction of the tip, $E_{local}(V_G)$ (V/cm) is

the local electrostatic field at the emitter tip, $A_{FN} = q^3/(8\pi h)$ and $B_{FN} = (8\pi/3)/(\sqrt{2m}/qh)$ where q is the electronic charge, h is Plank's constant, and m is the electron's effective mass, and $t(y)$ and $v(y)$ are the Nordheim elliptic functions where $y = \sqrt{q^3 E_{local}/4\pi\varepsilon_o\varphi^2}$ and ε_o is the electrical permittivity of free space. The Nordheim elliptic functions can be approximated as $t(y)$= 1.1 and $v(y)=0.95-y^2$ [10]. The local electric field is related to the applied voltage V_G through $E_{local}(V_G) = \beta.V_G$ where β (cm^{-1}) is the field factor. Therefore, Eq. 1 can be rewritten as

$$I_E(V_G) = \alpha_{tip}\frac{1.27\times10^{-6}}{\phi}\cdot\exp\left[\frac{9.87}{\sqrt{\phi}}\right]\cdot\beta^2\cdot V_G^2\cdot\exp\left[-\frac{6.53\times10^7\cdot\phi^{3/2}}{\beta\cdot V_G}\right] \text{ (A)} \qquad (2)$$

The field factor β relates the bias voltage to the surface electrostatic field and it is to first order equal to the inverse of the tip radius r. A better estimate for the field factor is given by [11],[12]

$$\beta = \frac{k_F}{r^n} \text{ (cm}^{-1}\text{)} \qquad (3)$$

where $k_F \approx 2.5\times10^6$, $n \approx$ 0.69-0.8, and r (nm) is the tip radius. Due to the exponential dependence on the field factor and hence the tip radius, emission currents are extremely sensitive to tip radii variation. Unfortunately, nanometer-sized tip radii in FEAs have a distribution with long tails such as Gaussian, lognormal, or Poisson [12]- [15]. Therefore, spatial variation of the tip radius results in the spatial variation of the emission current and hence the current density. It also results in non-uniform turn-on voltages even for tips that are located next to each other.

Figure 1 is a log-log plot depicting a family of IV characteristics from a single tip for an FEA that has a tip radii distribution with average radius r_o and radius variation Δ_r. Each emitter current falls within the turn-on limit (controlled by the noise floor) and the burn-out limit (due to Joule heating). For a constant bias voltage only a small fraction of the field emitters in the array emits electrons because the sharper tips burn out early, before the duller tips emit, resulting in under-utilization of the FEA. Attempts to increase the emission current by increasing the voltage often result in emitter burnout and

shifting of the operating voltage to higher voltages. Even though burning-out of the sharper tips of the FEA results in less emitter size variation and hence better emission uniformity, the larger average tip radius requires a larger bias voltage to produce the same current.

Consequently, alternative approaches for achieving uniform emission from FEAs have focused on control of the supply of electrons to the surface. In a metal the supply of electrons is very high, making the control of the supply challenging. However, in a semiconductor, where the local doping level and the local potential determine the concentration of electrons, it is possible to configure the emitter such that either the supply process or the transmission process determines the emission current. Emission uniformity by controlling the supply of electrons to groups of emitters using ungated field effect transistors (FETs) or MOSFETs as ballasting elements have been reported in the literature [16]-[18]. However, these approaches are not ideal because emission non-uniformity would still occur within the sub-set of emitters controlled by the same ballasting element. Individual control of the supply of electrons to each emitter would prevent destructive emission from the sharper tips while allowing higher overall current emission because of the emission of duller tips. Ballasting of individual emitters has not been attempted due fabrication complexity. Furthermore, individual ballasting of Si emitters using classical MOSFETs results in small density of emitters per unit of area.

We recently proposed to use vertical ungated FETs to individually control the emission of Si or CNT field emitters in an array to achieve uniform and high current [19]. This paper further explores the proposed technology by providing a comprehensive analytical background. Section II introduces the idea of individually ballasting field emitters with ungated FETs and presents a sensitivity analysis as metric for evaluating the effectiveness of this approach to achieve uniform emission. Section III reports the fabrication process and device simulations of the ungated FET, and the design of the individually ballasted field emitters. Section IV discusses the results of the simulations. Finally, Section V summarizes the findings.

II. INDIVIDUAL BALLASTING OF FEAS

A. Ballasting using linear resistors vs. FETs

The conventional approach to attain uniform electron emission from arrays of field emitters has been through the use of large feedback resistors in series with the field emitters. However, this approach is unattractive because low spatial current spread is achieved at the expense of the current level, as shown in Figure 2-A. A device that has current source-like behavior would be able to simultaneously provide high current and high dynamic resistance, making it an ideal ballasting element to implement spatially uniform FEAs. The ungated FETs act as current sources, effectively providing high current with high dynamic resistance for voltage drops across the FET larger than the saturation voltage, as shown in Figure 2-B. I_D, i.e., the current through an ungated FET, depends on the carrier concentration n, the electronic charge q, the drift carrier velocity v_d, and the cross-sectional area of the device $A(y)$, which in general is a function of the position along the channel y due to the variation in the surface depletion layer when a drain-to-source voltage V_{DS} is applied. The drift velocity is a function of the mobility μ and the electric field E_y, which is a derivative of the channel potential V_c. Therefore, the drain current I_D of the ungated FET is

$$I_D = A(y)\cdot q\cdot n\cdot \mu\cdot \frac{dV_c}{dy}\ (\mathrm{A}) \tag{4}$$

where the mobility μ is a function of E_y, the mobility at low fields μ_o, and the carrier saturation velocity v_{sat}

$$\mu = \frac{\mu_o}{\sqrt{1+\left(\frac{\mu_o}{v_{sat}}\right)^2\left(\frac{dV_c}{dy}\right)^2}}\ (\mathrm{cm^2V^{-1}s^{-1}}) \tag{5}$$

The surface depletion layer increases from the source end to the drain end of the ungated FET; therefore, the channel cross-sectional area $A(y)$ decreases from the source end to the drain end. Since the carrier concentration is constant, conservation of charge implies that the electron

velocity and hence the electrostatic field increases from the source to the drain. For a certain drain-to-source bias voltage V_{DSS}, the channel will pinch off while the carrier velocity will reach its saturation value v_{sat}, resulting in a drain saturation current I_{DSS}. If V_{DS} is further increased, the depletion layer in essence grows towards the source resulting in the reduction of the effective channel, typically termed channel length modulation. Consequently, there is a gradual increase in the drain current I_D with applied drain-to-source voltage beyond V_{DSS}. This behavior can be modeled as a linear increase in the drain current for drain-to-source voltages beyond V_{DSS}

$$I_D \cong I_{DSS}\left[1+\lambda\left(V_{DS}-V_{DSS}\right)\right] = I_{DSS} + g_{out}\left(V_{DS}-V_{DSS}\right) \text{ (A)} \tag{6}$$

where λ is the channel length modulation parameter and g_{out} (Ω^{-1}) is output conductance of the FET in the saturation regime. As shown in Section III, both high saturation current and high output resistance are achievable with the right combination of doping level N_D and device geometry. A high aspect-ratio single-crystal Si column is a two-terminal ungated FET that can be fabricated using both deep reactive ion etching (DRIE) and thermal oxidation. The two-terminal vertical ungated FET can easily be integrated with FEAs to create dense arrays of individually ballasted field emitters that emit spatially uniform high currents, as shown in Figure 3. The FET acts as current limiter for the FET/FE structure.

B. Sensitivity Analysis

The sensitivity S is a measure of the emitter current variability across the array and it is defined as the ratio of maximum emission current variation ΔI_E and the average emission current $\bar{I}_E$

$$S = \frac{\Delta I_E}{\bar{I}_E} = 2\frac{I_{MAX}-I_{MIN}}{I_{MAX}+I_{MIN}} \tag{7}$$

where I_{MAX} and I_{MIN} are the maximum and minimum emitter currents of the FEA respectively. Examining Eq. 2, the current coming out of a field emitter has two independent sources of variability: (i) the work function can vary due to absorption/desorption of gases, and (ii) the tip radius can vary across

the emitter array. Therefore, the current sensitivity S of the FET/FE unit is defined in terms of the variations in the workfunction and the tip radius as

$$S = S_{\phi} + S_r = \frac{1}{I_E}\frac{\partial I_E}{\partial \phi}\Delta\phi + \frac{1}{I_E}\frac{\partial I_E}{\partial r}\Delta r \tag{8}$$

where S_{*} and S_r are the current sensitivities with respect to the variations in the workfunction and the tip radius, and $\Delta\phi$ and Δr are the variations in workfunction and tip radius respectively. In this discussion we shall assume that temporal changes in the field-emitted current are due to temporal fluctuations in the workfunction (i.e., $\phi = \phi(t)$), and spatial non-uniformities in the field-emitted current are due to spatial variations of the tip radius (i.e., $r = r(\vec{R})$). Using Eqs. 2 and 6 the emission current from a FET/FE unit is equal to the implicit function

$$I_E(V_G) = \alpha_{tip}\frac{1.27\times10^{-6}}{\phi}\cdot\beta^2\cdot\left(V_G - V_{DSS} - (I_E - I_{DSS})\cdot r_{out}\right)^2\cdot\exp\left[\frac{9.87}{\sqrt{\phi}} - \frac{6.53\times10^7\cdot\phi^{3/2}}{\beta\cdot\left(V_G - V_{DSS} - (I_E - I_{DSS})\cdot r_{out}\right)}\right] \text{ (A) (9)}$$

where r_{out} is the output resistance of the FET. The implementation of a FET-based individual electron supply control in an FEA can decrease both the temporal and spatial non-uniformities. However, this work focuses on the non-uniformities in current emission due to spatial variation. Using Eqs. 9 and 3, the variation of the emitter current on the tip radius is

$$\frac{dI_E}{dr} = -\frac{\frac{2n}{r} + \frac{6.53\times10^7\cdot\phi^{3/2}\cdot n\cdot r^{n-1}}{k_F\cdot\left(V_G - V_{DSS} - (I_E - I_{DSS})\cdot r_{out}\right)}}{\frac{1}{I} + \frac{2r_{out}}{\left(V_G - V_{DSS} - (I_E - I_{DSS})\cdot r_{out}\right)} + \frac{6.53\times10^7\cdot\phi^{3/2}\cdot r_{out}\cdot r^n}{k_F\cdot\left(V_G - V_{DSS} - (I_E - I_{DSS})\cdot r_{out}\right)^2}} \text{ (A/cm)} \tag{10}$$

We used Eqs. 8 – 10 to estimate the emission current and the radius-dependent sensitivity S_r of an ungated FET/FE basic unit and the results are shown in Figure 4. In these estimations a total bias voltage V_G of 100 V was applied across the series combination of the FE and the FET, with $\alpha_{tip} = 0.4\pi\cdot r^2$, r_o = *30 nm*, Δr *= 5 nm*, ϕ *= 4.05 eV*, $I_{DSS} = 1\mu A$, and the output resistance was varied between 10^2 Ω and 10^{10} Ω. From this analysis, an output resistance larger than 100 MΩ is needed to achieve a sensitivity smaller than 1 for a tip emitting 1 μA.

III. UNGATED FET PROCESS AND DEVICE SIMULATION

Based on a desired sensitivity S =1, extensive process and device simulations of high aspect-ratio silicon columns were conducted using the SILVACO software (Silvaco International, Santa Clara CA). The ungated FET cross-sectional area was set at 1 μm × 1 μm, while the channel length was varied between 10 and 100 μm and the doping concentration was varied between 10^{13} and 10^{16} cm^{-3}. From these simulations critical device parameters were extracted. Figure 5 shows the maximum current, saturation current, linear conductance, and output conductance as a function of the doping concentration N_D for a 1 μm × 1 μm × 100 μm ungated FET. We also explored the dependence of the linear resistance, output resistance, maximum current, and saturation current on the channel length for an ungated FET with a fixed doping concentration and cross-section. From Figure 6 it can be inferred that the functional dependence of the linear and output resistance on the channel length is not the same (otherwise, the data would describe parallel lines in the plot); from the same figure we can also infer that the FET has as a current source-like behavior only when the aspect-ratio of the FET is larger than about 50.

IV. DISCUSSION

Figure 7 illustrates the performance of the ungated FET / FEA structure and the ability of the FETs to increase the total output current of the FEA by protecting the sharper emitters from burning-out. For this simulation it was assumed that the saturation current of the FET is 5×10^{-7} A, the burn-out current is 1×10^{-6} A, and that the FEA is composed of field emitters with tip radii that have Gaussian with nominal tip radius 30 nm and standard deviation 5 nm. As seen on Figure 7, for low bias voltages the IV characteristics of the FET/FEA structure is equivalent to the IV characteristics of the FEA with no supply control structure. However, for large bias voltages, the weighted IV characteristics of the FET/FEA structure saturates to a value close to the FET current saturation. A FEA biased at a voltage that produces current emission above the burn-out value would lose a portion of its elements due to

Joule heating. The net result of the burn-out is a weighted IV characteristics with a shift in the operational voltage and lower current emission for the same bias voltage. From Eq. 2 it can be inferred that the IV characteristics of an electron source that obeys the FN model describe a straight line in a FN plot, i.e., a plot of ln (I/V_G^2) vs. V_G^{-1}. However, an individually ballasted FEA has a FN plot that for large enough bias voltages the slope decreases until it becomes horizontal or even positive, as shown in Figure 8. Based on the analysis and simulations presented in this section, we estimate that ungated FETs with substantially larger aspect ratios than the ones proposed by Takemura et al [17] are required to achieve good spatial emission uniformity.

A potential drawback of the field emission array that is individually ballasted by ungated FETs is the spread in energy of the emitted electrons. Energy spread results from the variation in the tip radius and hence the gate to emitter voltage required to obtain the particular emission current imposed by the current limiter. There are several approaches to mitigate against the spread in energy of the emitted electrons. One approach will be to operate the device at the space charge limit. Another approach would be to lower the operating voltage and hence the energy spread by scaling the tip radius and the gate aperture to smaller dimensions in order to increase the field factor β.

V. SUMMARY AND CONCLUSION

We demonstrated through simulations that large arrays Si field emitters can achieve high and uniform electron current emission if each field emitter is individually controlled (ballasted) by an ungated FET. The ungated FET achieved current source-like behavior due to the velocity satuarion of electrons in silicon, the very high aspect-ratio of the ungated FET, and the doping concentration. We proposed individually ballasted FEAs composed of FET/FE units where the field emitter is fabricated on top of a vertical ungated FET (a high aspect-ratio silicon column) to maximize the FEA emitter density.

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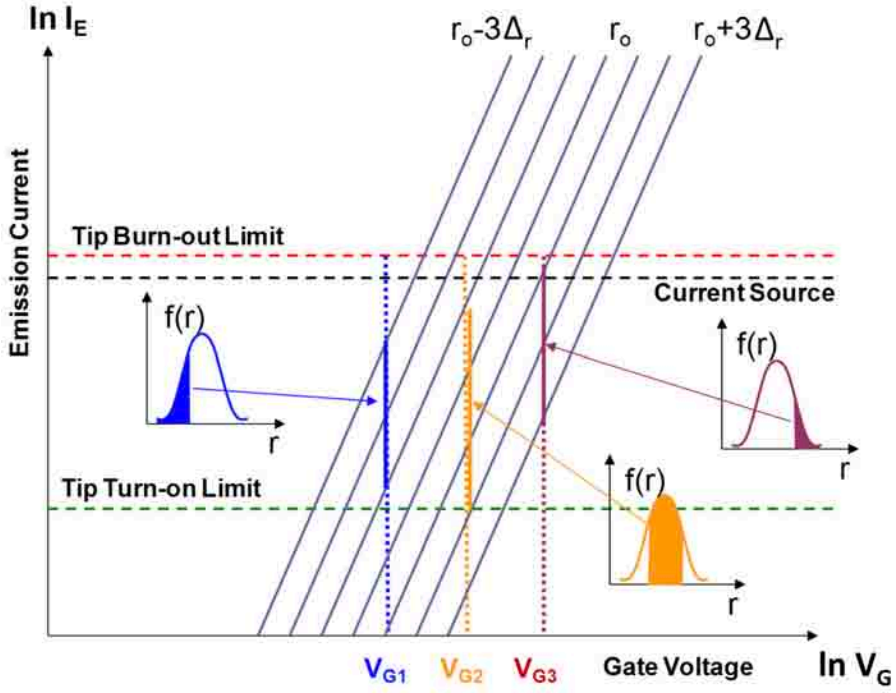

Figure 1 *Log-log plot of the emission current I_E versus gate voltage V_G for varying tip radii r. For a constant gate bias voltage, only a small fraction of the tip array emits current.*

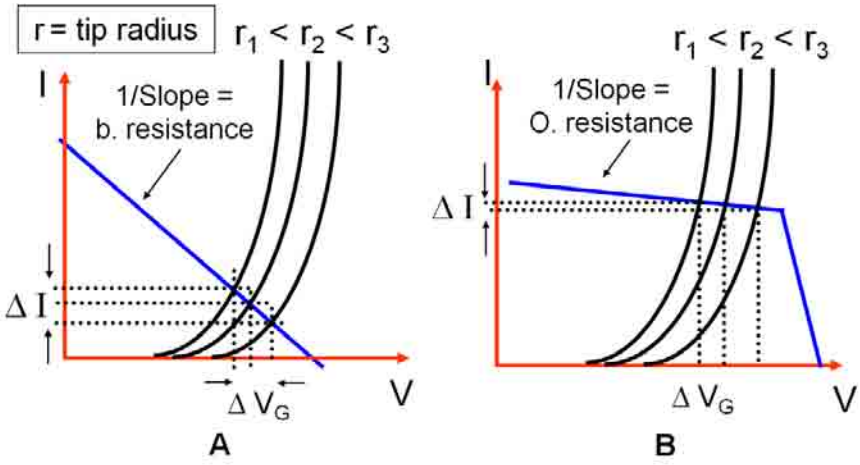

Figure 2 *Negative feedback of a field emitter using a linear resistor (A) and an ungated FET (B). In the first case, low emission current variation within the FEA is achieved using a very large linear resistance, which results in low-current emission. If an ungated FET is used instead, both low variation and high-current emission are achieved because the current uniformity depends on the magnitude of the output resistance of the FET, which is independent of its saturation current.*

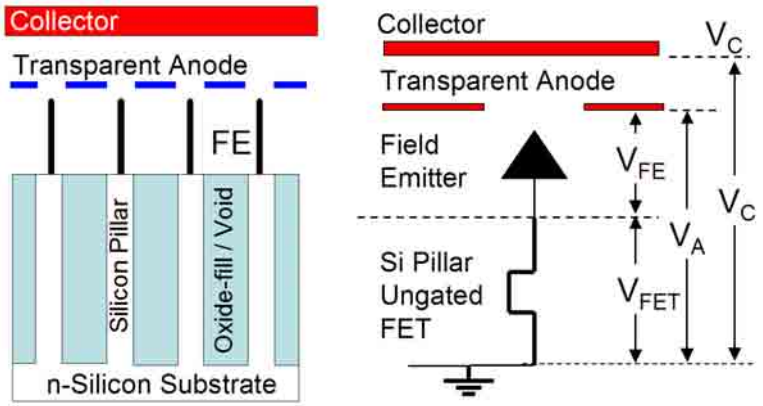

Figure 3 *Device structure (left) and equivalent circuit (right). Each field emitter (FE) is formed on top of a different silicon column (i.e., ungated FET). The bias voltage V_A is divided between the voltage across the FE, i.e., V_{FE}, and the voltage across the FET, i.e., V_{FET}.*

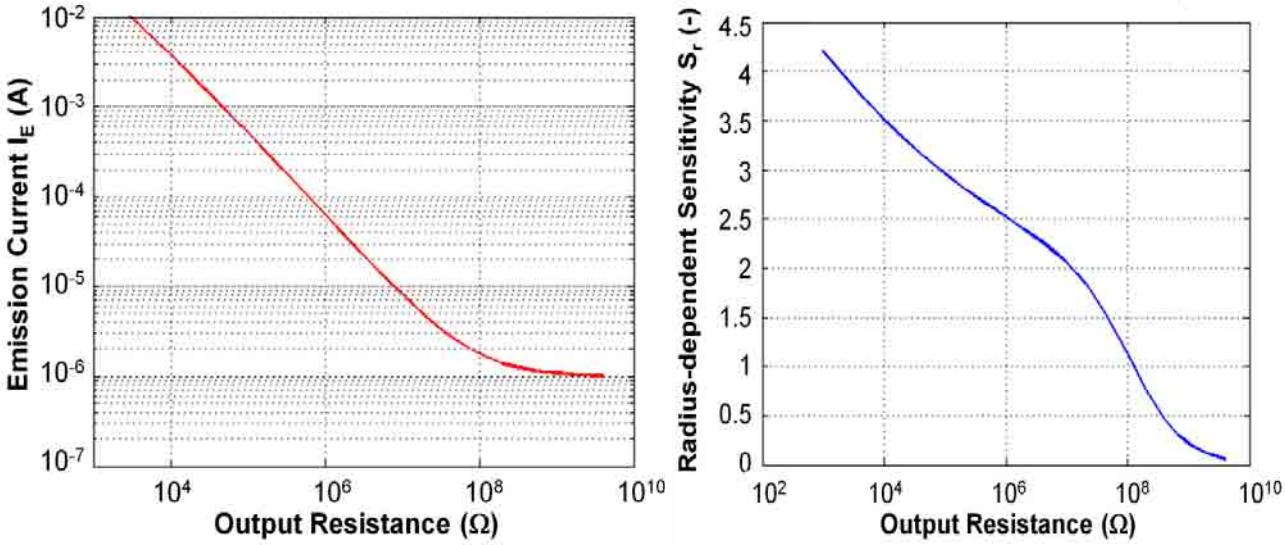

Figure 4 *Emission current (left) and radius-dependent sensitivity S_r (right) for an FET/FE unit.*

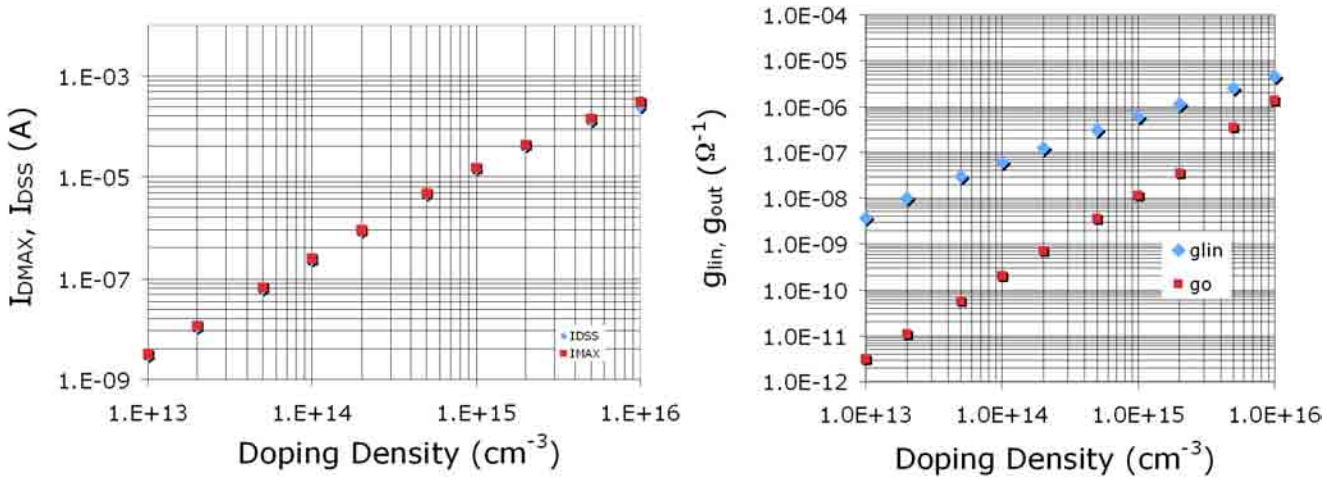

Figure 5 *Drain-source saturation current I_{DSS} and maximum current @ 100 V I_{DMAX} (left), and linear conductance g_{lin} and output conductance g_{out} (right) vs. doping concentration for a 1 μm × 1 μm × 100 μm ungated Si FET.*

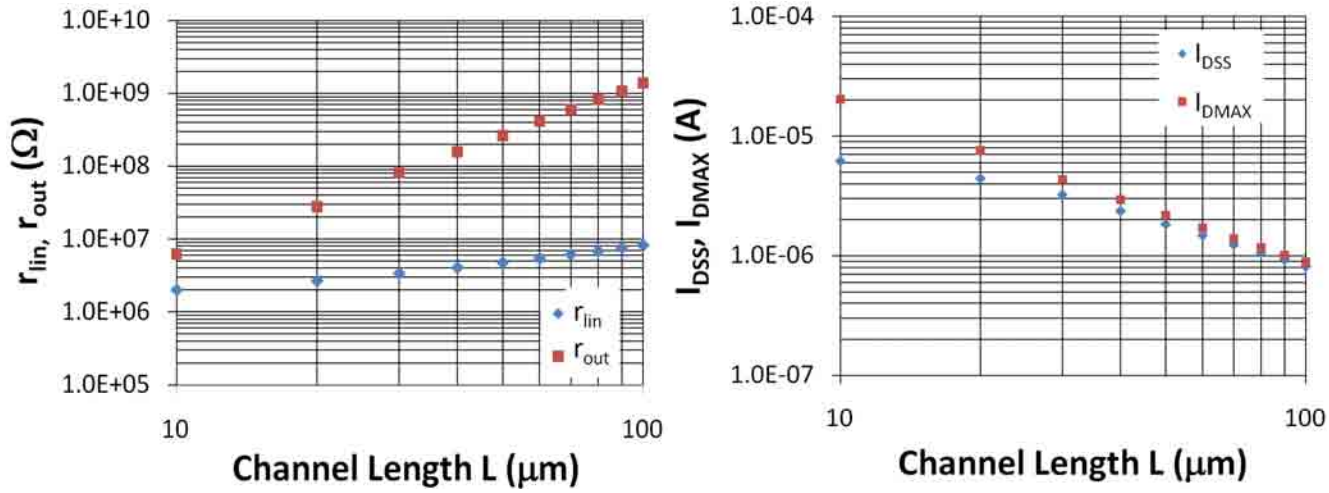

Figure 6 *Linear resistance r_{lin} and output resistance r_{out} (left), and saturation current I_{DSS} and maximum current I_{DMAX} (right) vs. channel length for an ungated FET with 1* μm × *1* μm *cross-section and 2×10^{14} cm^{-3} doping concentration.*

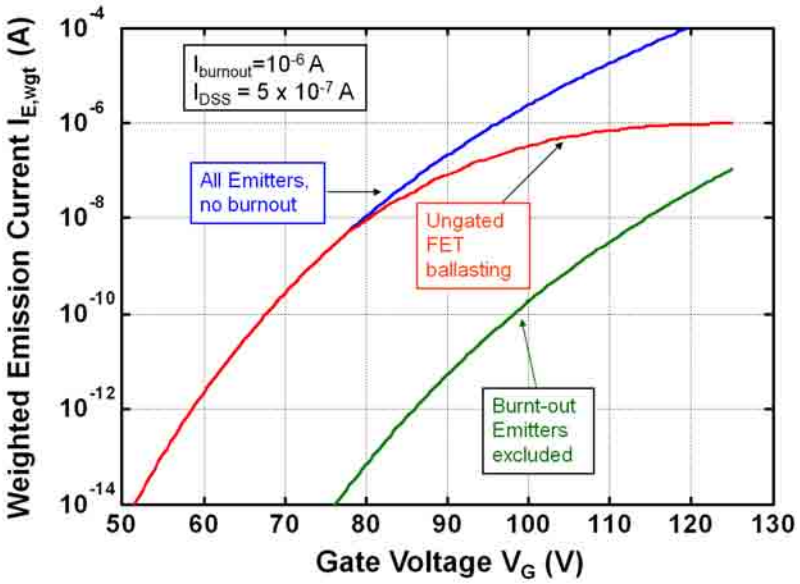

Figure 7 *Weighted IV characterisitcs of an FET / FEA structure,weighted IV charactersitics of the FEA if no FETs are present and no emitter burn-out occurs, andweighted IV characteristics of the FEA if no FETs are present and emitter burn-out occurs.*

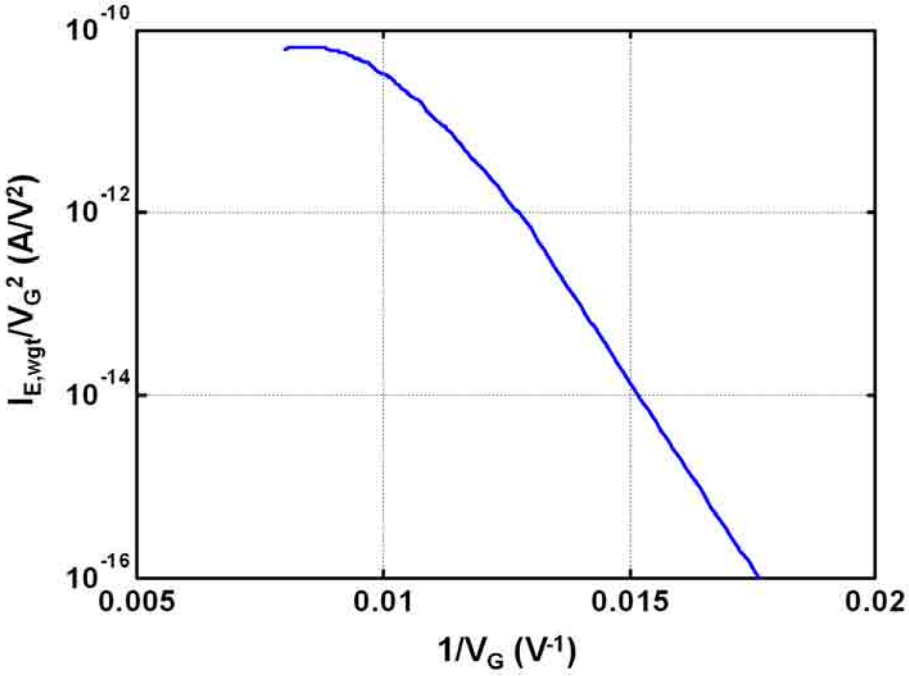

Figure 8 *For low bias voltage, the weighted IV characterisitcs of an individually ballasted FEA describe a straight line in the FN plot. For large bias voltages, the current limitation by the FETs forces the slope of the FN plot to decrease until it becomes horizontal. Further increase of the bias voltage will make the slope become positive.*

Uniform High-Current Cathodes Using Massive Arrays of Si Field Emitters Individually Controlled by Vertical Si Ungated FETs – Part B: Device Fabrication and Characterization

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***Abstract*—We report the demonstration of electron sources that achieve high current and uniform emission using dense arrays of Si field emitters that are individually ballasted by a current source. Each field emitter is fabricated on top of a vertical ungated field effect transistor (FET), a two-terminal device based on a very high aspect-ratio Si column. The ungated FET takes advantage of the velocity saturation of electrons in silicon, the high aspect-ratio of the ungated FET, and the doping concentration to achieve current source-like behavior, to obtain reliable uniform and high-current electron emission. Emitted currents in excess of 0.48 A were demonstrated.**

***Index Terms*—Ballasting, cathodes, electron supply control, Si field emission arrays, vertical ungated Si FETs.**

I. INTRODUCTION

Field emission cathodes are an attractive alternative to thermionic electron sources because they are less power-hungry, potentially more reliable, faster, and more compatible with portable applications. Field emission arrays (FEAs) could be used in a variety of vacuum micro- and nano-electronic device applications such as field emission displays (FEDs), high frequency amplifiers, gas ionizers, X-ray sources, and multi-electron beam lithography [1]-[6]. In the majority of these applications current level, stability, reliability, lifetime, and emission uniformity are the key metrics for cathode performance. Field emission of electrons from metal or semiconductor surfaces consists of two processes: (i) transmission of electrons (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by the application of a high electrostatic field, and (ii) supply of electrons from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the field emitter (FE). Control of the transmission process to produce high uniform current from FEAs has largely been unsuccessful because of the exponential dependence of field emission current on the emitter tip radius [7] and the long-tail distribution of nano-sharp field emitter arrays [8]-[11]. Consequently, alternative approaches for achieving uniform emission from FEAs have focused on control of the supply of electrons to the surface. In a metal the supply of electrons is very high, making the control of the supply challenging. However, in a semiconductor, where the local doping level and the local potential determine the concentration of electrons, it is possible to configure the emitter such that either the supply process or the transmission process determines the emission current. Emission uniformity by controlling the supply of electrons to groups of emitters using ungated field effect transistors (FETs) or MOSFETs as ballasting elements has been reported in the literature [12]-[14]. However, these approaches are not ideal because emission non-uniformity would still occur within the sub-set of emitters controlled by the same ballasting element.

We recently proposed to use vertical ungated FETs to individually control the emission of Si or CNT

field emitters in an array to achieve uniform and high current [15]. The ungated FET takes advantage of the carrier velocity saturation in silicon, the very high aspect-ratio of the ungated FET, and the doping concentration to achieve current source-like behavior. In Part A of this article, we showed through simulations that the control of electron emission from individual field emitters using ungated FETs can span a wide range of emission current per tip and also achieve full current limitation of the FEA [16]. In Part B of this article, we provide experimental proof that arrays of Si field emitters individually ballasted by vertical ungated FETs are capable of uniform and high electron current emission. Section II reports the fabrication of arrays of Si field emitters that are individually controlled by a vertical ungated FET. Section III reports and analyzes the experimental data of the individually ballasted FEAs, clearly showing that the FETs control the current emission. Section IV discusses the results. Finally, Section V summarizes the findings.

II. FABRICATION

Large arrays of field emitters (10^6 emitters in 1 cm^2) that are individually controlled by vertical ungated FETs were fabricated to demonstrate large and uniform field emission currents. The fabricated devices have no integrated extraction gate and hence an external perforated grid provided the extraction field. The process flow to fabricate the arrays of field emitters individually controlled with vertical ungated FETs uses 6-inch n-Si wafers and it is shown in Figure 1, while Figure 2 is a collage of SEMs at different stages of the fabrication. First, the substrates are coated with a thin film stack (a 0.5 μm PECVD SiO_2 film on top of a 0.5 μm LPCVD silicon-rich silicon nitride film on top of a 0.5 μm thermal SiO_2 film). Then, the thin film stack is etched using contact photolithography and reactive ion etching (RIE) to form arrays of 1,000 × 1,000 squares 3.5 μm wide spaced 10 μm. After that, a deep reactive ion etching (DRIE) step with no passivation commences the FE sharpening. Next, the vertical ungated FETs are etched using DRIE (Figure 2-A). Finally, the wafers are RCA cleaned and oxidized to form massive

arrays of nano-sharp tips (Figure 2-B) on top of columns about 1 μm × μm × 100 μm (Figure 2-C).

III. EXPERIMENTAL RESULTS

A. Individually ballasted FEAs, DC IV Characteristics

We were able to obtain evidence of current limitation from arrays of Si field emitters individually controlled by ungated FETs that were tested at high DC voltages in vacuum (10^{-9} Torr). The characterization of large FEAs made of silicon with a doping concentration below 2×10^{14} cm^{-3} showed a substantial degree of electron supply control.

Experimental setup: Arrays of 1-million Si field emitters individually ballasted by vertical ungated FETs (1 cm^2 of emitting area) were fabricated as described in Section II using silicon wafers with resistivity values that span two orders of magnitude of doping concentration (10^{13} – 10^{15} cm^{-3}). The FEAs were tested using the setup shown in Figure 3. In the setup, a global unaligned perforated grid was placed in close proximity of the emitter tips using a thin (~ 25 um-thick) polymer gasket that acted as stand-off between the substrate and the grid. When a voltage is applied between the grid and the FEA, electrons are field emitted from the FEA and a fraction of which is transmitted through the transparent grid. There is a 2 mm diameter metallic sphere suspended about 5 millimeters above the grid that was used as an external collector. The collector was biased at + 1100 V. The objective of using a collector is to allow us discriminate between leakage current through the dielectric and electron emission. If there is a linear dependence between the current collected by the grid (grid current I_G) and the current collected by the suspended electrode (collector current I_C), we can conclude that both currents have the same physical origin. Since the suspended electrode has no physical contact with the FEA, the origin of the measured currents cannot be leakage current through the polymer gasket. We also conducted reverse-polarity tests to verify that the measured current was field emitted, and we verified that the current emitted by the FEA (I_E) was equal to the grid current plus the collector current. Also, we conducted FN analysis of the data to verify that the FEA was the origin of the measured

currents. We used a set of Keithley 237s controlled by Labview to collect the IV characteristics of the arrays of field emitters individually controlled by vertical ungated FETs. The instruments are able to measure a maximum current of 10 mA and apply a bias voltage between -1100 and 1100 V.

Highly doped substrates, low-current: A field emitter individually controlled by an ungated FET is in essence a potential divider with the voltage applied between the grid and the ground, i.e., V_G, divided between the voltage drop between the grid and the field emitter, i.e., V_{GE}, and the voltage drop between the drain and the source of the ungated FET, i.e., V_{DS}. Emission current from a single field emitter that is individually ballasted will be limited when the voltage drop across the FET is such that the ungated FET is operating in its current saturation region, i.e., the drain-to-source voltage drop across the FET is greater than its corresponding saturation voltage ($V_{DS} \geq V_{DSS}$). The saturation current of a 1×1×100 um vertical ungated FET with a doping concentration of 1×10^{15} cm^{-3} is about 14 uA (Figure 4), while the maximum emission current that can be measured using the DC testing setup is 10 mA, which corresponds to 10 nA per tip if the emission is evenly distributed. Therefore, the IV characteristics from an individually ballasted FEA made of highly doped silicon should show no deviation from the expected FN behavior. In this case, the current I_E from a field emitter due to a bias voltage V_G is given by the FN equation [7]

$$I_E(V_G) = \alpha_{tip} \frac{1.27\times10^{-6}}{\phi} \cdot \exp\left[\frac{9.87}{\sqrt{\phi}}\right] \cdot \beta^2 \cdot V_G^2 \cdot \exp\left[-\frac{6.53\times10^7 \cdot \phi^{3/2}}{\beta \cdot V_G}\right] \text{ (A)} \qquad (1)$$

where ϕ is the workfunction of the tip, α_{tip} is the area of the tip involved in the emission, and β is the field factor of the tip. The field factor relates the electrostatic field at the surface of the tip to the bias voltage. A semi-empirical expression to estimate β is [17]

$$\beta = \frac{k_F}{r^n} \text{ } (cm^{-1}) \qquad (2)$$

where $k_F \approx 2.5\times10^6$, $n \approx$ 0.69-0.8, and r (nm) is the tip radius. Figure 5-A shows the IV characteristics of a 1-million FEA made of silicon with a doping concentration of about 1×10^{15} cm^{-3}. The device emits

current above the noise floor for voltages larger than 125 V, and a maximum total emission current of about 100 μA. Figure 5-B clearly indicates a linear dependence between the collector current and the grid current (the collector current is about 2.4% the grid current with a correlation R^2>0.995), which suggests that the measured currents are field emitted. As shown in Figure 5-C, the FN plots of the grid and collector currents are parallel lines with an average slope that corresponds to a field factor β of 2.34×10^5 cm^{-1} if a workfunction of 4.05 eV is assumed for Si. Using Eq. 2 with $k_F = 2.5 \times 10^6$ and n = 0.69 results in an estimated tip radius of about 31 nm. From Figure 5-D, the typical tip radius from SEMs is about 51 nm. As expected, the tip radius from the FN plot is smaller than the typical tip radius from SEMs because only the sharper tips of the tail end of the FEA distribution are emitting.

Lowly doped substrates, low-current: A large FEA emits low current most likely because the applied bias voltage is only able to turn-on a few emitters of the array rather than because all the emitters are contributing to the emission. The emitters that are active will most likely have similar tip radii, resulting in a narrower tip size distribution and a similar behavior that could show a substantial deviation from the expected FN behavior before more emitters turn-on and contribute to the total current output. We experimentally confirmed that even for relatively small current levels (<1 mA) individually ballasted FEAs made with lowly doped silicon exhibit IV characteristics that show a substantial degree of electron supply control. For example, Figure 6-A shows the IV characteristics of a 1-million FEA made of silicon with a doping concentration of about 2×10^{13} cm^{-3}. The device emits current above the noise floor for voltages larger than 200 V, and a maximum total emission current of about 145 μA was measured. Figure 6-B clearly indicates a linear dependence between the collector current and the grid current (the collector current is about 1% the grid current with a correlation R^2>0.995), which suggests that the measured currents are field emitted. As shown in Figure 6-C, the FN plots of the grid and collector currents at low voltage are two parallel straight lines. However, for voltages above 575 V the FN plots clearly show a decrease of the slope due to the current regulation of the FETs. Using the slope of the linear part of the FN plots we estimate a field factor β of 1.3×10^5 cm^{-1}

using 4.05 eV as the workfunction for Si. Using Eq. 2 with $k_F = 2.5 \times 10^6$ and n = 0.69 results in an estimated tip radius of about 72.5 nm. From Fig. Figure 6-D, the average tip radius from SEMs is about 87 nm. As expected, the typical FEA tip radius from SEMs is larger than the tip radius from the FN plot because at low-current emission only the sharper tips are emitting. We should note that the FN slope was extracted at low extraction grid voltages in which emission current will be dominated by tips with radii much smaller than the average tip radius. For the doping level of the device, the saturation current per emitter from simulations is about 10 nA as shown in Figure 4. Therefore, roughly about 14,500 emitters (1.45% of the FEA) were active while the FEA emitted 145 μA during the test.

We can obtain an estimate of the tip radii variation based on the tip radius from the FN plot, the tip radius from the SEMs, and the estimate of the fraction of the FEA that was active if we assume a Gaussian tip radii distribution. We expect the typical tip radius from SEMs to be close to the average tip radius of the distribution because in a symmetrical statistical distribution the mode of the distribution is equal to its mean [18]; we also expect the tip radius from the FN plot to be representative of the array of field emitters that was active. A Gaussian distribution of a variable x can be normalized (i.e., mean equal to 0 and standard deviation equal to 1) if we use the transformation $Z = (x - \bar{x})/\sigma$, where σ and $\bar{x}$ are the standard deviation and the mean of x, respectively. Therefore, we estimated the variation in the tip radius Δ_r as

$$\Delta_r = \frac{r_{FN} - r_{SEM}}{Z}; \quad \%FEA_{ON} = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{Z} \exp\left(-\frac{\theta^2}{2}\right) d\theta \tag{3}$$

where Δ_r is the estimated tip radii variation, r_{FN} is the tip radius from the FN plot, r_{SEM} is the typical tip radius from SEMs, $\%FEA_{ON}$ is the percentage of the FEA that was active, and Z is the value of the normalized variable that corresponds to a cumulative Gaussian distribution equal to $\%FEA_{ON}$. Using Eq. 3 we obtain Δ_r = 6.6 nm, i.e., i.e., $r_{FN} = r_{SEM} - 2.19\Delta_r$. Therefore, the tip radii variation is about 7.5% the average tip radius.

B. Individually ballasted FEAs, Pulsed IV Characteristics

While conducting the DC experiments, we observed that the heat dissipated by the grid due to current interception limited the maximum emission current that could be sustained by the polymer gasket. We observed that at current levels above 1 mA the heat dissipated by the grid reflowed the polymer gasket, which resulted in a lower voltage required to achieve the same emission current in subsequent tests. Eventually the gasket shorted for devices that continuously emitted mA-level currents. As an estimate, 10 mA of emission current at a gate bias of 1000V dissipated 10W. Since most of the current is intercepted by the grid, most of the 10 W would heat up the grid (about 2.5 W/cm^2, comparable to the power density of a wafer helium-cooled reactive ion etcher). This level of heat dissipation should reflow the gasket. To avoid sustained heat dissipation while characterizing the FEAs, we implemented a pulsed setup. The setup also enabled us to obtain substantially larger emission currents, as well as to demonstrate complete current saturation at high voltage from an individually ballasted FEA made of silicon with a doping concentration of 2.4×10^{13} cm^{-3}.

Experimental setup: A block diagram of the pulsed test rig is shown in Figure 7. It is based on the DC test setup shown in Figure 3, which is composed of the individually ballasted FEA, an unaligned perforated grid separated by a polymer gasket, and an external collector. In the pulsed test rig the FEA is connected to the ground through a resistor R_M that is used to determine the current emitted by the FEA. The grid voltage is supplied by a Glassman EQ1R1200 power supply that is controlled by a DEI PVX-4140 pulse generator. The collector electrode voltage is supplied by a Glassman LH3R1.721 power supply. Pulses of 2 μs with a period of 10 s were used to energize the grid. We verified that the pulse duration is long enough to produce a steady-state response from the FEAs, while the square wave period is long enough to substantially decrease the impact of the grid heat dissipation. We also verified the linearity between the collector current and the emitted current.

Medium doped substrates, high-current: Figure 8-A is a plot of the DC and pulsed IV characteristics of a 1-million array of field emitters individually ballasted by ungated FETs that was fabricated on a

silicon substrate with a resistivity of 34.7 Ω.cm (doping concentration of 1.25×10^{14} cm^{-3}). The maximum emitted current per tip is 0.48 uA assuming uniform operation of the FEA. This is consistent with the maximum current I_{MAX} = 0.4 uA obtained at a bias of 100 V from simulations of the FET (Figure 4). The FN plot of the emitted current obtained from both DC and pulsed tests is shown in Figure 8-B. The plot clearly shows that for high grid voltage, the emission current is electron supply limited whereas for lower applied grid voltages the emission current is barrier limited. In the electron supply limited regime, the emitted current of 0.48 A is consistent with the saturation current of the ungated FET is one allows for the finite output resistance of the ungated FET. From the section of the FN plot for which electron emission is barrier limited, we estimated a field factor equal to 2.26×10^{5} cm^{-1} using 4.05 eV as the workfunction for Si; the field factor corresponds to a tip diameter of 32.5 nm if one uses Eq. 2 with $k_F = 2.5 \times 10^6$ and n = 0.69. The radius estimate is consistent with the tip radius of 42 nm from SEMs as shown in Figure 9. We should note that the FN slope was extracted from data at low extraction grid voltages in which the emission current is dominated by tips with radii smaller than the average tip radius.

Lowly doped substrates, high-current: Figure 10-A is a plot of the DC and pulsed IV characteristics for an array of 1-million field emitters individually controlled by vertical ungated FETs that was fabricated on a substrate with a resistivity of 178 Ω.cm (doping concentration of 2.4×10^{13} cm^{-3}). The emission current saturates at 0.109 A at grid voltages above 1200 V. The maximum emission current per tip is 109 nA, which is a factor of 5 larger than the 20 nA saturation current from simulations of the FET (Figure 4). Given the output conductance of the ungated FET, it is expected that the emission current will vary with the voltage drop across the ungated FET especially for the sharper tips. It is not clear at this time if this would account for the almost factor of 5 larger emission current per tip than the simulated ungated FET. Another potential source of additional current for the ungated FET is impact ionization at the drain region of the ungated FET due to the high voltage between the source and the drain. Also, impurity segregation into the silicon channel is expected to increase the channel doping,

which should substantially increase the carrier concentration in lowly-doped substrates. The FN plot of the emitted current obtained from both the DC and pulsed tests is shown in Figure 10-B. At low voltages, the slope of the FN plot is constant and negative, corresponding to the region dominated by electron transmission through the barrier. However, the slope becomes positive at high voltages (> 1200 V) corresponding to the region dominated by electron supply to the barrier, as previously shown by Hong et al for FEAs ballasted by a MOSFET [14]. From the region in which electron emission is controlled by transmission through the barrier we extracted field factor equal to 2.73×10^5 cm^{-1}, which corresponds to a tip radius if 24.8 nm if we use Eq. 2 with $k_F = 2.5 \times 10^6$ and $n = 0.69$. This is consistent with the tip radius of 33 nm from the SEMs as shown in Figure 11. We should note that the FN slope was extracted from data at low extraction grid voltages in which the emission current is dominated by tips with radii smaller than the average tip radius.

IV. DISCUSSION

Very little has been reported in the literature on two-terminal current limiters. In order to obtain current limitation resistors or transistors are often used with the added need to bias the third terminal. The earliest two-terminal current limiter reported in the literature was by Boll et al which used diffused contacts into Germanium to obtain current source like behavior from an gated FET structure. They attributed the current limitation to the saturation of velocity in Ge [19]. Baek et al reported work on ungated GaAs MESFET structure which has essentially the same structure at Boll et al with the exception that the substrate is now GaAs and the contacts were ion implanted [20]. Again, Baek et al explained their results using velocity saturation of carrier in GaAs. This work builds on the results reported by Boll and Baek which used very closed spaced contacts in order to attain high fields and hence saturation velocity at relatively small voltages. This work also invokes velocity saturation of carriers. However, in this case the contacts are not closely spaced but rather the contacts are spaced much further apart. Velocity saturation is attained by pinching off the channel at the drain end by the

drain-to-source voltage. Pinch off is easily attained for a Si column with narrow width i.e. high aspect ratio column. Using a wider column leads to a higher drain voltage for the channel to pinch-off.

When the Si column ungated FET is integrated with the field emitter, we observe that the emitted current is limited by the ungated FET. This is consistent with prior work on the control of emission current from field emitter arrays by transistors [14] and the other preceding literature reports by Itoh [21], Kanemaru [22], and Nagao [23]. Takemura et al reported a silicon current limiter based on trench etching of Si, oxide filling, and planarization [12]. However, they did not attempt to control emission current form individual emitters. When the current limiter is used with a group of field emitters, it provides current limitation at high current levels. This is consistent with the fact that the current limiter did not have high aspect-ratio and the columns cross-sectional area was relatively big (4 μm x 4 μm). This means that the current through the columns will only saturate at very high current levels. Using the work reported by Takemura et al, Imura et al reported remarkable reliability from the FEAs and were used in a demonstration of very high-performance travelling wave tubes (TWTs) [24]. The silicon columns provided current limitation to an array of FE at very high current levels thus enhancing reliability of the array. The current limiters enhance reliability at the array level but do not necessarily prevent burnout of the sharpest emitter tips within the array nor enhance uniformity. The high currents are well above the operating regime of the tubes. Our device provides individual current limitation to each tip using a high aspect ratio silicon column resulting in uniform and reliable field emitter arrays.

We have operated field emitter arrays that are individually ballasted for periods longer than 20 hours. The device operated at the instrument current compliance limit of 10 mA with an applied gate to emitter voltage >600 V. Since the 95% of the emitted current was intercepted by the gate, this implies than about 5.5 W was dissipated in the structure resulting in a temperature increase and partial melting or softening of the spacer which led to the reduction in the spacing between the gate and the emitter and consequently an increase in the current until current compliance in the instrument was reached. This eventually resulted in a short between the gate and the emitter. However, each time the spacer was

replaced and the device went back to approximately the same operating conditions after adjusting for changes in spacer thickness. There was never any evidence of emitter tip burn-out from Joule heating suggesting that the Si column ungated FET was effective in limiting current through the field emitter. More systematic study of the effect of the Si column current limiter on the emitter tip lifetime needs to be conducted.

V. CONCLUSIONS

We demonstrated high-current electron sources that achieve uniform emission using large and dense arrays of individually ballasted Si field emitters. Each field emitter is fabricated on top of a vertical ungated FET. The ungated FET achieves current source-like behavior due to the velocity saturation of electrons in silicon, the very high aspect-ratio of the ungated FET, and the doping concentration. Evidence of full ballasting was provided. Emitted currents in excess of 0.48 A were demonstrated.

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Figures

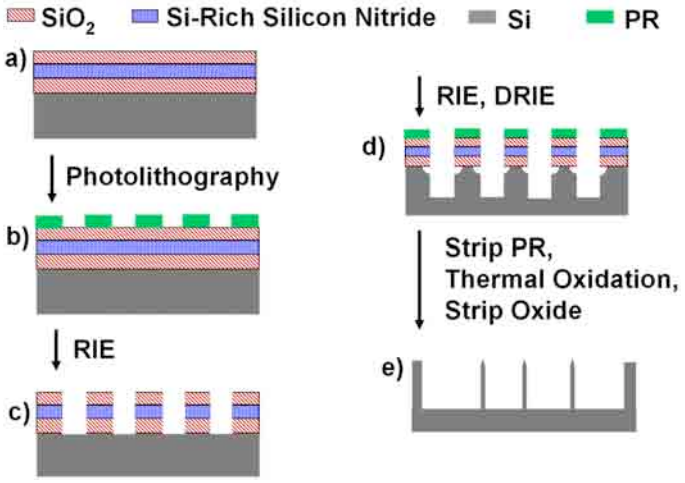

Figure 1 *Process flow to fabricate arrays of field emitters individually controlled by vertical ungated FETs.*

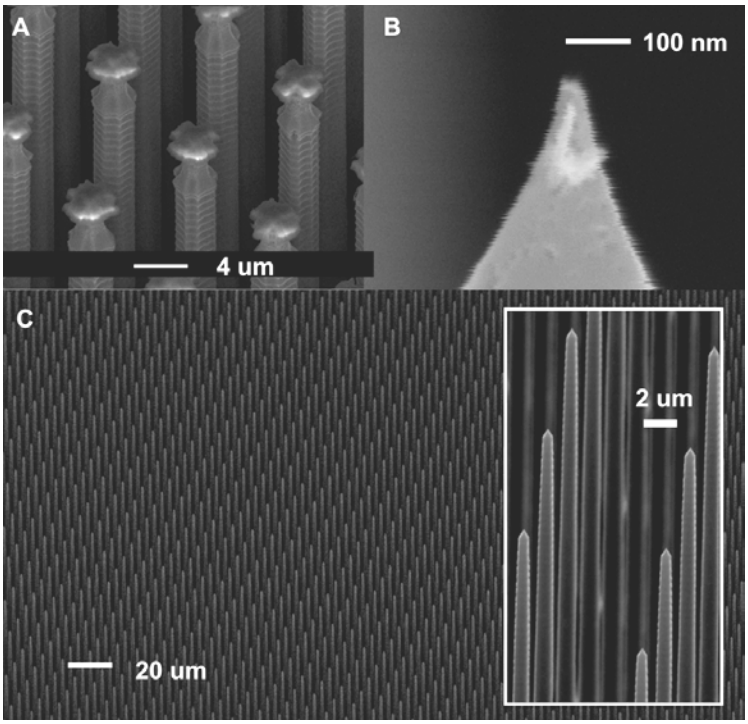

Figure 2 *Selected images of the process flow to fabricate individually ballasted FEAs using vertical ungated FETs: DRIE of the vertical ungated FETs with partically sharpened Si field emitters (A); close-up of an emitter tip after full sharpening (B); field view of a large FEA and close-up of the final FET/FE structure (C).*

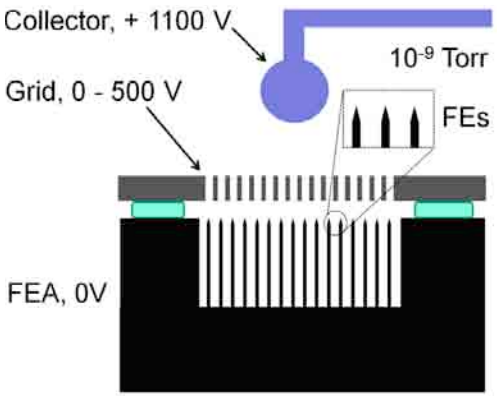

Figure 3 *Schematic of the transparent grid diode setup used to test the individually ballasted FEAs. In the DC tests, the FEA, grid, and collector were energized using three Keithley 237.*

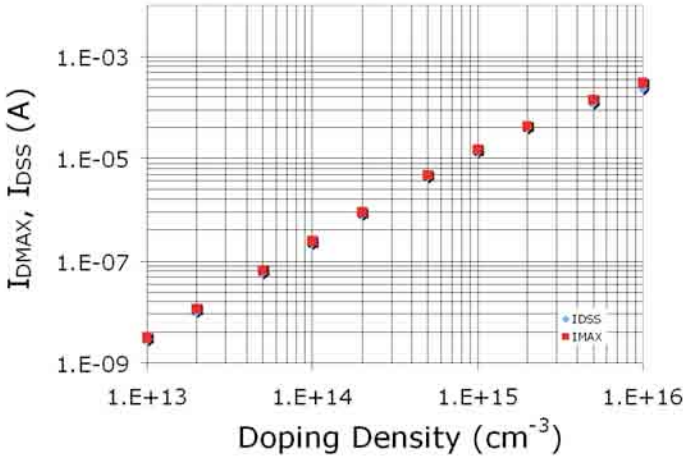

Figure 4 *Drain-source saturation current I_{DSS} and maximum current @ 100 V I_{DMAX} vs. doping concentration for a 1 μm × 1 μm × 100 μm ungated Si FET.*

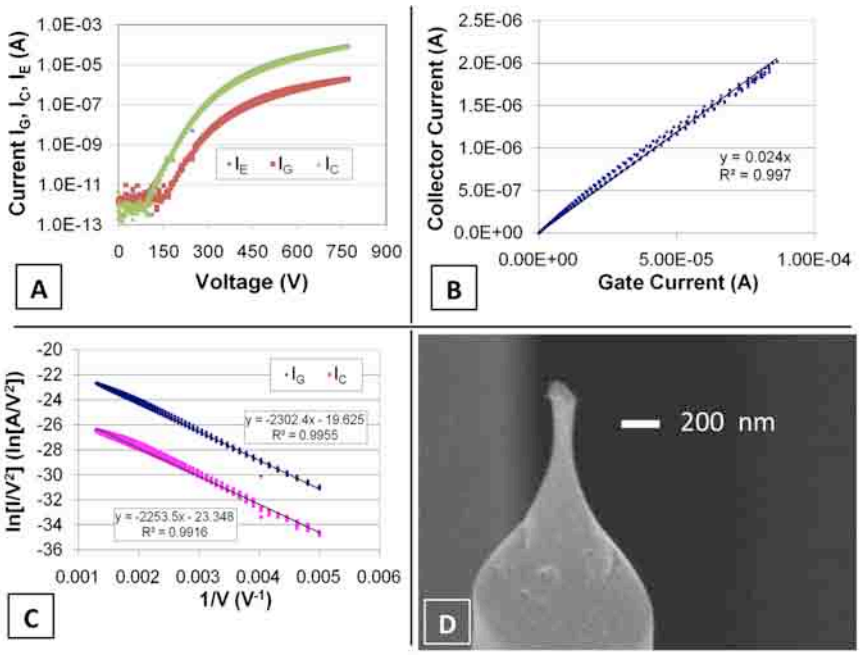

Figure 5 *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made with highly doped silicon: IV characteristics (A), collector current vs. Gate current (B), FN plot of the grid current and collector current (C),and SEM of a typical FE (D).*

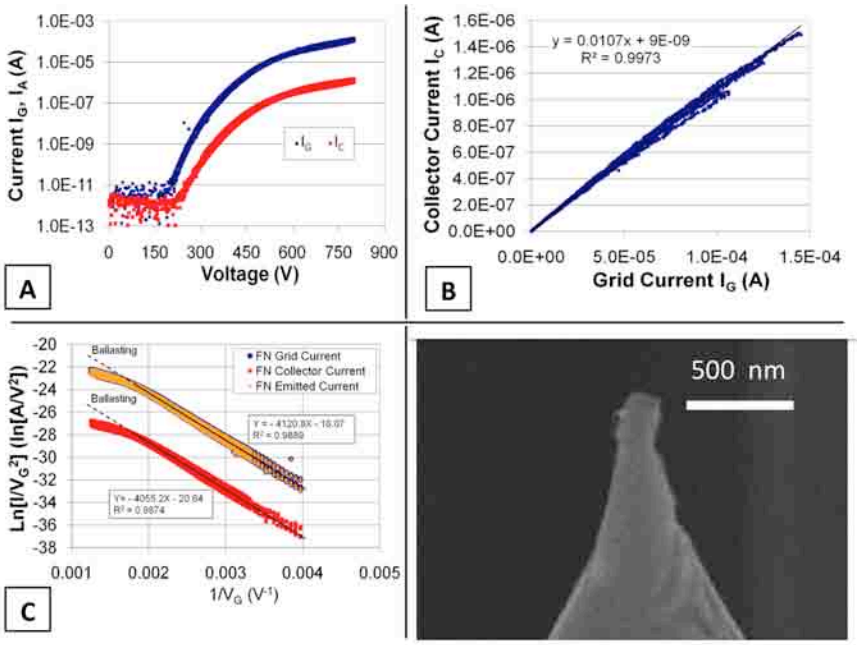

Figure 6 *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made of lowly doped silicon: IV characteristics (A), collector current vs. Gate current (B), FN plot of the grid current and collector current (C),and SEM of a typical FE (D).*

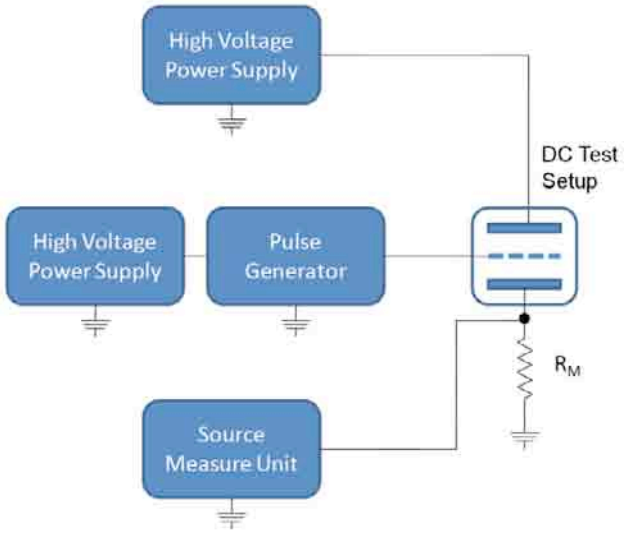

Figure 7 *Block diagram of the pulsed DC setup.*

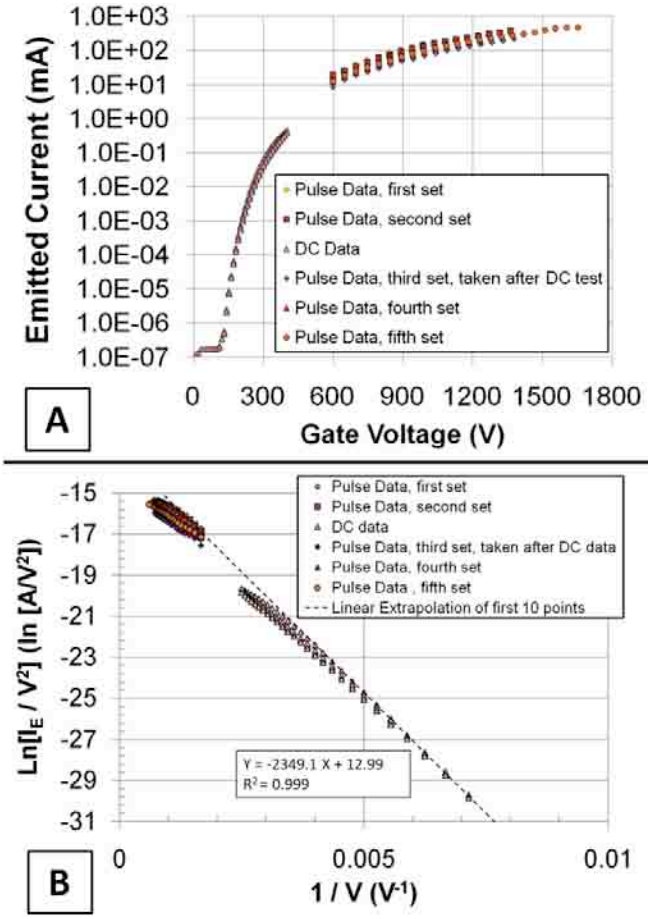

Figure 8 *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made of silicon with a resistivity of 34.7 Ω.cm: IV characteristics (A), FN plot of the emission current (B).*

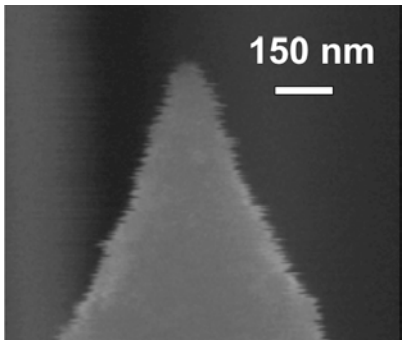

Figure 9 *SEM of a typical field emitter part of the the individually ballasted FEA made of silicon with of 34.7 Ω.cm resistivity. The tip radius is about 43 nm.*

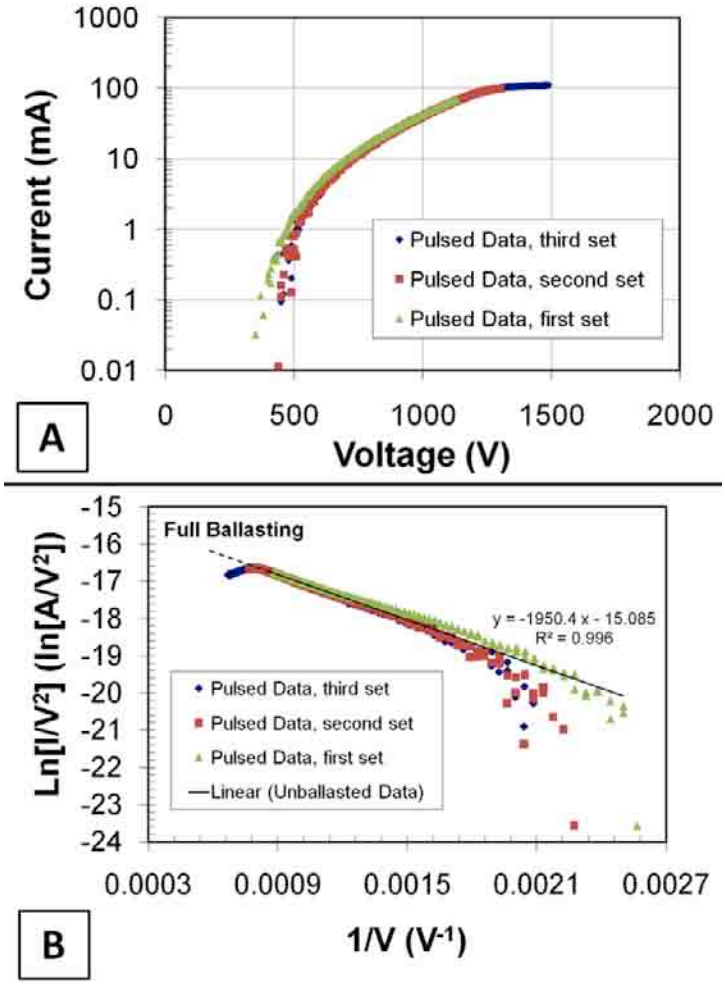

Figure 10 *Characterization of a 1-million array of field emitters individually controlled by ungated FETs made of silicon with a resistivity of 178 Ω.cm: IV characteristics (A), FN plot of the emission current (B).*

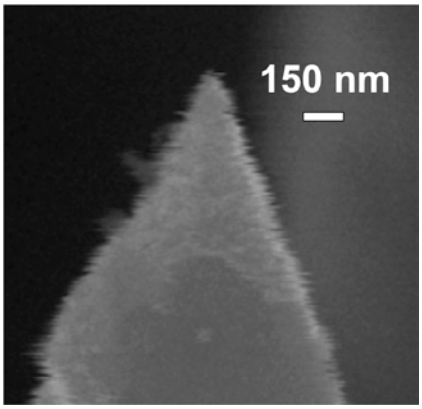

Figure 11 *SEM of a typical field emitter part of of the individually ballasted FEA made of silicon with 178 Ω.cm resitivity. The tip radius is about 33 nm.*